

# Digital techniques for real-time pulse shaping in radiation measurements

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## Abstract

Recursive algorithms for real-time digital pulse shaping in pulse height measurements have been developed. The differentiated signal from the preamplifier (exponential pulse) is amplified and then digitized. Digital data are deconvolved so that the response of the high-pass network is eliminated. The deconvolved pulse is processed by a time-invariant digital filter which allows trapezoidal/triangular or cusp-like shapes to be synthesized. A prototype of a digital trapezoidal processor was built which is capable of sampling and processing digital data in real time at clock rates up to 50 MHz.

## 1. Introduction

In our previous work [1] we described recursive algorithms for real time pulse processing in high resolution spectroscopy. In that paper we also proposed a hardware configuration for a trapezoidal/triangular pulse shaper. Although we presented some initial results obtained using a quasi-real time system, our further work has now resulted in the assembly and testing of a prototype that operates in true real time.

In the discussion that follows, it is assumed that an exponential pulse is digitized. This signal can be obtained by CR differentiation of the signal from a reset type charge sensitive preamplifier or by differentiation with a pole-zero cancellation network of the signal from a resistive feedback preamplifier. This approach allows elimination of the dc offset of the preamplifier signal and sufficient amplification of the short exponential pulses so that maximum utilization of the resolution of the sampling ADC can be achieved. We also include processing algorithms assuming a digitized step input signal. This situations holds when the output of a reset type preamplifier is directly digitized. In this case, the digital resolution of the signal and the number of samples per convolution window [2].

The practical realization of digital processors depends on the complexity of the algorithms they implement. Because of their suitability for real-time implementation, our initial efforts have concentrated on the use of two digital shaping algorithms [1]. The first allows symmetrical trapezoidal/triangular pulse shapes to be synthesized. The

# 2. Trapezoidal digital pulse-shaper

The recursive algorithm [1] that converts a digitized exponential pulse v(n) into a symmetrical trapezoidal pulse s(n) is given as

$$d^{k,l}(n) = v(n) - v(n-k) - v(n-l) + v(n-k-l),$$
(1)

$$p(n) = p(n-1) + d^{k,l}(n), \quad n \ge 0,$$
(2)

$$r(n) = p(n) + Md^{k,l}(n),$$
 (3)

$$s(n) = s(n-1) + r(n), \quad n \ge 0,$$
 (4)

where v(n), p(n), and s(n) are equal to zero for n < 0. The parameter *M* depends only on the decay time constant  $\tau$  of the exponential pulse and the sampling period  $T_{clk}$  of the digitizer, and is given by

$$M = \frac{1}{\exp(T_{\rm clk}/\tau) - 1}.$$
(5)

For values of  $\tau/T_{\rm clk} > 5$ , Eq. (5) can be approximated as  $M \approx \tau/T_{\rm clk} - 0.5$ .

Eq. (1) can be expressed as a consequence of two identical procedures given by the set of equations

$$d^{k}(n) = v(n) - v(n-k),$$
(6)

$$d^{k,l}(n) = d^k(n) - d^k(n-l).$$
(7)

The unit that implements the algorithm of Eq. (6) or Eq. (7) is depicted in Fig. 1. We call this building block a

second algorithm transforms an exponential or step pulse to a symmetrical pulse shape with the leading edge proportional to  $t^2 + t$ . We call this shape "cusp-like."

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Fig. 1. Block diagram of the delay-subtract unit

delay-subtract unit (DS), and it consists of two functional elements: a programmable delay pipeline and a subtracter. It is clear that the algorithm given by Eq. (1) can be realized by connecting two DS units in series. The delay pipeline of one of the units has a depth of k while the depth of the pipeline of the other is l. Since each of these units represents a linear time-invariant system, the order of connection of the units is insignificant. Under such circumstances, the duration of the rising (falling) edge of the trapezoidal shape is given by the smaller value of k and l(min(k, l)) and the duration of the flat part of the trapezoid



Fig. 2. Block diagram of the high-pass network digital deconvolver.



Fig. 3. Digital pole-zero cancellation configuration.

is given by the absolute value of the difference between k and l (abs(l-k)).

One of the most important components of the digital trapezoidal shaper is the unit which performs the operations given by Eqs. (2) and (3). The algorithm determined by these equations deconvolves the response of CR highpass filter. In other words, if a sampled exponential pulse with decay time constant  $\tau$  is applied to the input of such a unit, the response is a step signal. Fig. 2 shows a block diagram of the high-pass filter deconvolver (HPD). The multiplication parameter M is again given by Eq. (5). It is important to note that the HPD unit can be placed any-where along the processing chain of the time-invariant trapezoidal shaper. However, if it is connected before the delay-subtract units, the output data accumulate for each processed pulse and eventually will cause an overflow in the arithmetic circuit.

The HPD unit can also be used as a digital pole-zero cancellation circuit. Since both the HPD and CR differentiation networks are linear time-invariant systems the combined response of both units connected in series is independent of the order of connection. Thus, the effect of the input exponential pulse can be eliminated by setting the parameter M as a function of the decay time constant of the input signal (Eq. (5)). An example of a digital pole-zero cancellation circuit is shown in Fig. 3.

The last building block of the trapezoidal/triangular shaper is an accumulator which implements the algorithm given by Eq. (4). This unit is placed last in the processing chain. The digital resolution of the accumulator should be sufficient to accommodate the maximum possible digital value of the output data.

Using the building blocks described above, we have built a prototype of the trapezoidal/triangular digital shaper. The prototype was assembled as two printed circuit boards, approximately  $10 \times 10$  cm. The power consumption of the processor (excluding sampling ADC) is about 5 W. The maximum clock speed of the circuit is 50 MHz. All the parameters of the shaped signal are digitally controlled.

A block diagram of the digital trapezoidal shaper is shown in Fig. 4. When the input signal is a step function, the HPD unit is bypassed. In this case, the digital data after



Fig. 4. Block diagram of the digital trapezoidal/triangular shaper The elements are:  $DELAY_n - a$  delay pipeline,  $\Sigma_n - an$  adder/subtracter,  $ACC_n - an$  accumulator,  $X_n - a$  multiplier.





Fig. 5. Oscillograms of triangular and trapezoidal shapes at the output of a DAC connected to the digital pulse shaper. The upper trace in each of the oscillograms is the input exponential pulse. The time base is set to 2  $\mu$ s per division.

two operations of delay-subtract are directly applied to the output accumulator. In order to allow the processor to accept either exponential or step input signals, a modified version of the HPD unit was used. The accumulator in Fig. 2 was replaced with a multiplier-accumulator as in Fig. 4. The input data of the multiplier and the multiplier accumulator are multiplied by two coefficients  $m_1$  and  $m_2$  respectively.

When the input signal is an exponential pulse, the relationship between the multiplier coefficients  $m_1$  and  $m_2$  is given by

$$m_1/m_2 = M, \tag{8}$$

where  $m_2$  is a parameter that determines the digital gain of the shaper and M is given by Eq. (5). When the input signal is a step function, the coefficient  $m_2$  is zero and the digital gain is determined by the multiplier coefficient  $m_1$ . The adjustable digital gain is an important feature that allows matching of the range of the shaper output data to the range of the multichannel memory.

In order to display the real-time operation of the digital shaper, a digital-to-analog converter (DAC) was connected at the output of the shaper. The output data were truncated so that the upper 12 bits of the shaped signal were used. The processor was tested using a 12 bit ADC operating at 20 MHz. The input exponential signal and the reconstructed analog signal from the DAC were displayed on the screen of an analog oscilloscope. Fig. 5 shows examples of the response of the shaper to an exponential pulse.

## 3. Cusp-like digital pulse shaper

Two algorithms for cusp-like digital pulse shaping using a step input signal were presented in Ref. [1]. The first recursive algorithm allows only a pulse with a sharp peak to be synthesized. The second algorithm is more complex, allowing adjustment of the duration of a flat top on a truncated cusp-like pulse. Due to its relative simplicity, the first algorithm can easily be implemented in hardware.

We have developed a model of the hardware configuration which operates according to the recursive algorithm given as

$$d^{k}(n) = v(n) - v(n-k),$$
(9)

$$p(n) = p(n-1) + d^{k}(n), \quad n \ge 0,$$
(10)

$$s(n) = s(n-1) + p(n) - v(n-l)k, \quad n \ge 0,$$
(11)

where v(n) is the digitized input signal and s(n) is the response of the shaper. It is again assumed that v(n), p(n), and s(n) are equal to zero for n < 0. The delay parameter l determines the duration of rising and falling edges while the parameter k depends on l as k = 2l + 1. An additional equation, which describes the response of an



Fig. 6. Block diagram of the digital cusp-like shaper.



Fig. 7. Simulated pulse shapes at different points of the cusp-like shaper.

HPD unit, can be attached to this algorithm so that the shaper can process exponential pulses.

The major problem associated with the algorithm given by Eqs. (9)–(11) is that p(n) gradually increases after each processed pulse. Thus, after certain number of processed pulses the accumulator performing the algorithm of Eq. (10) saturates. To avoid numerical overflow at any one of the building modules of the cusp-like shaper a modified set of equations can be used. This modified algorithm, including the response of an HPD unit, can be written as

$$d^{k}(n) = v(n) - v(n-k),$$
(12)

$$d^{1}(n) = v(n) - v(n-1),$$
(13)

$$p(n) = p(n-1) + d^{k}(n) - kd^{1}(n-l), \quad n \ge 0, \quad (14)$$

$$q(n) = q(n-1) + m_2 p(n), \quad n \ge 0,$$
(15)

$$s(n) = s(n-1) + q(n) + m_1 p(n), \quad n \ge 0.$$
 (16)

The parameters  $m_1$  and  $m_2$  relate to each other according to Eq. (8):  $m_1/m_2 = M$ . As in the case of the trapezoidal shaper, the digital gain can be controlled using these two parameters.

A block diagram of a cusp-like digital shaper is depicted in Fig. 6. Most of the building blocks are similar to those used in the trapezoidal shaper. A digital differentiator is built using the one-clock delay register and an arithmetic unit  $\Sigma_2$ . The input signal can be either a step or exponential pulse. Multiplier coefficients  $m_1$  and  $m_2$  serve the same function as described for the trapezoidal shaper.

The function of the circuit was tested using a computer generated exponential signal. The response of the cusp-like shaper and the signal shape at different points of the configuration are presented in Fig. 7. Note that the signal is bipolar at the intermediate points of the circuit. Hence, the possibility for an overflow is eliminated.

#### 4. Conclusion

Efficient algorithms for real-time digital pulse-shaping have been developed. Based on these algorithms two configurations of linear time-invariant shapers have been investigated and tested. The first allows trapezoidal/ triangular pulse shapes to be synthesized. The prototype operates at clock rates up to 50 MHz and allows full digital control of the shape parameters. The second configuration generates cusp-like, finite duration pulses. Both digital shapers can accept either step or exponential input pulses, and the selection is digitally (software) controlled.

#### References

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