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A multi-channel integrated circuit for use in low- and intermediate-energy nuclear physics—HINP16C

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Abstract

The design, simulations, and tests of a 16-channel chip for solid-state detectors are presented. The chip produces sparsified pulse trains for both linear (pulse height) and timing (relative to an external reference) and allows the use of one of two internal charge sensitive amplifiers or an external amplifier. A shaper and peak detector are implemented in the linear branch and a pseudo-constant fraction discriminator and time-to-voltage converter are implemented in the logic/timing branch. The internal plus external gain options and the preparation of both pulse height and timing pulse trains suitable for pipeline ADCs, makes the chip suitable for a wide variety of applications. The chip was fabricated in the AMI 0.5 μm n-well (C5N) process available through MOS implementation services (MOSIS).

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1. Introduction

The need for high-density signal processing in the low- and intermediate-energy nuclear physics communities is widespread. However, the typical channel count (usually no more than a few thousand) has thus far not risen to the level deemed necessary for chip development. While the current menu of multi-channel integrated circuits (IC) is substantial, there exist no chips with large dynamic range and actual energy range (>50 MeV), good timing resolution, self-triggering with on-chip sparsification, and the capability to handle very large capacitance. The latter is needed, for example, to service thin dE detectors used in particle identification telescopes. (Capacitances in excess of 200 pF are not unusual.)

In view of the above, we have designed and built an IC which accomplishes all the above, in part by allowing use with an external charge-sensitive amplifier (CSA) in addition to an internal one (with two ranges). Either way, the user can couple the IC system to cost-effective pipeline ADCs. (The financial advantage of this is clear when one appreciates that the cost per channel of commercial ADCs are in the range of $ 150 per channel.)

The chip which we describe in this paper, which we call HINP16C, was designed to be used in the few thousand channel strip Si project called High-Resolution Array (for HiRA). A full paper on this project is presented elsewhere [1]. (A site where the full set of schematics for the HINP16C chip is also provided in Ref. [1].) The chip described here services the sixteen 32×32 strip double-sided Si E detectors and the sixteen 65 μm, 32 strip single-sided Si dEs of HiRA. To date the chip has been used in five experiments. These experiments made use of both the internal (for the E's) and external CSAs (for the dEs) and were run in both sparsified and all channel dump modes. The flexibility of this chip (the fact that it is not so "application" specific) allows other Si devices to make use

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of it and therefore experiments with intermediate channel counts can benefit from the cost savings of chip analog processing coupled with modern pipeline ADCs.

2. General description

The IC was fabricated in the AMI 0.5 μm n-well process (C5N) available through MOSIS (see www.mosis.org). This non-silicided CMOS process has 3 metal layers and supports double poly capacitors (1 fF/μm^2). It also has a high resistance (1 kΩ per square) poly layer.

Each of the 16 channels of the HINP16C consists of a charge sensitive amplifier (CSA) with two gain modes: high-gain (15 mV/MeV or 0.4 mV/fC) and low-gain (3 mV/MeV or 0.08 mV/fC). The high-gain mode is linear up to approximately 100 MeV while the low-gain mode is linear up to approximately 500 MeV. The CSA output is split to feed energy and timing branches, each of which produce sparsified pulse trains with synchronized addresses for off-chip digitization with a pipelined ADC.

The energy leg consists of a shaping filter with a fast return to baseline, <20 μs. This slow shaper is followed by a continuous-time peak sampling circuit. Simulated and measured (using a pulser) energy resolution is 38 keV with an ideal 75 pF load in the high-gain (100 MeV) mode.

The timing leg consists of a Nowlin pseudo-constant fraction discriminator (CFD) composed of a leading-edge and a zero-crossing discriminator. The zero-crossing discriminator has its offsets dynamically nulled. A 6-bit DAC is used to correct offsets associated with the leading-edge circuit as well as to set the CFD threshold levels.

When the CFD fires it starts a time-to-voltage converter (TVC). The TVC circuit has two (selectable) measurement ranges: 250 ns and 1 μs. The charging concludes with a common stop signal applied to all channels. The TVC circuit and the peak sampling circuit are automatically reset after a user-controlled variable delay time, referenced to when the CFD fires. To acquire the analog information, the user must supply a pulse to veto the reset. This veto thus selects an event for readout and digitization. A fast logical 'OR' signal and an analog output proportional to the number of channels that were hit, 'MULT', are available for off-chip high-level logical decisions and to decide, for example, if the veto reset is to be sent. The logical 'OR' and 'MULT' are also automatically reset unless vetoed by the user.

A central common channel provides biasing for the 16 processing channels and contains the readout electronics. A 48-bit configuration register allows the user to select: CSA gain/input option, processing for either positive or negative CSA pulses, TVC measurement range, a test mode (allowing CSA, Shaper and CFD inspection of any channel), to selectively disable CFD outputs on a channel-by-channel basis, and to assign an 8-bit ID to the chip. The chip only responds when an externally applied chip address matches the ID stored in the chip's configuration register.

3. The channel

The block diagram for each of 16 channels is illustrated in Fig. 1.

3.1. Charge-sensitive amplifier

The CSA is used to convert the charge packet, originating at the silicon-strip detector, into a voltage [2,3]. A single-ended folded cascode topology was used in the core amplfier. A source follower buffers the output [4]. The core amplifier used in the design of the CSA is presented in Fig. 2. A feedback capacitor, C_f (between the CF and IN nodes) sets the gain. A large feedback resistor

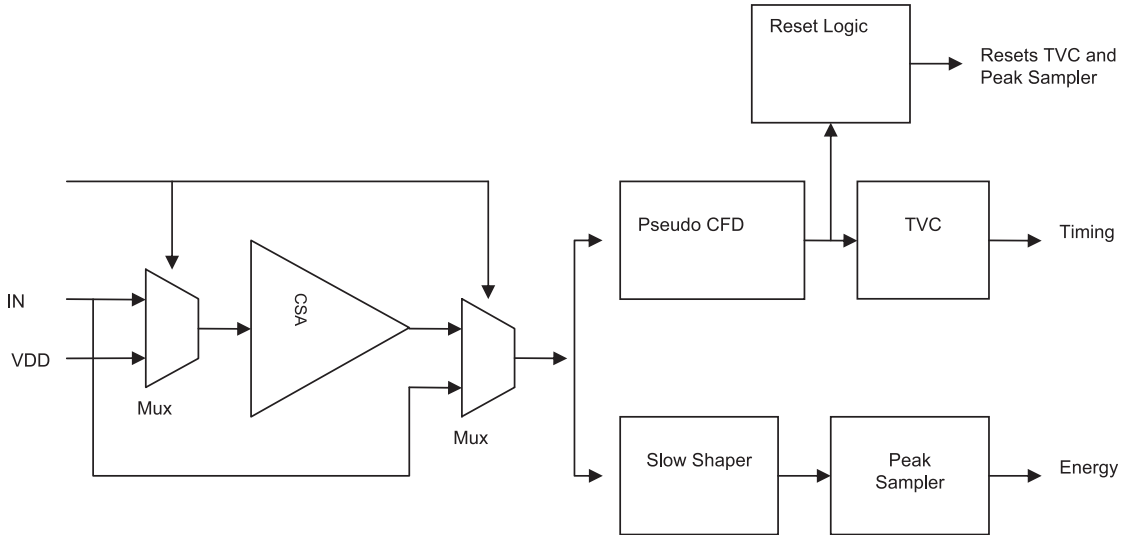

Fig. 1. Block diagram of a single channel. Each channel consists of a CSA followed by an energy and timing branch. The timing branch consists of a Nowlin CFD and a time-to-voltage converter (TVC) while the energy leg is comprised of a slow shaper and a peak sampling circuit.

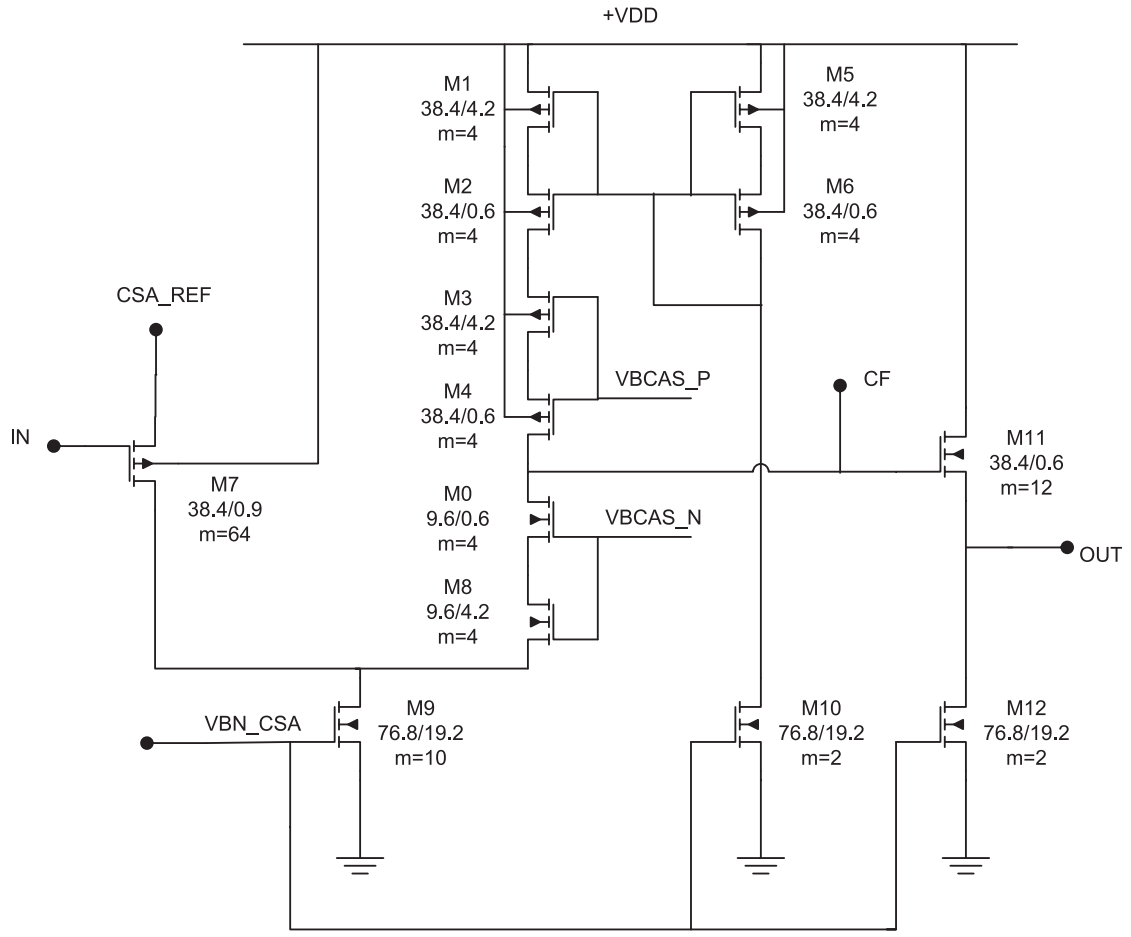

Fig. 2. Core amplifier used in CSA. The amplifier consists of a folded cascode and a source follower.

(between the OUT and IN nodes), implemented using a high-resistance polysilicon layer, effectively (but not directly) in parallel with the gain setting capacitor, determines the decay-time constant.

The CSA can be placed in one of two gain modes: C_f equal 2.5 pF (referred to as the high- gain mode) and C_f equal 12.5 pF (referred to as the low-gain mode). In the high-gain mode, the amplifier input PFET is biased with a 1 mA current. The decay time constant is nominally the same (25 μs) in both gain settings. Moreover, the internal CSAs can be bypassed and the downstream electronics can be driven by off-chip, external preamps. When this mode is selected, by setting the appropriate bit in an on-chip configuration register, the internal CSA is effectively shut down. The gate of the PFET input device is connected to the positive supply rail. This drives the output of the CSA near the negative rail.

3.2. Pulse shaper

The primary function of the pulse shaper circuit is to optimize the SNR of the detector readout system while providing a voltage proportional to the energy of the detected particle. The CSA output is fed to the pulse shaper, which acts as an integrator and stores the charge.

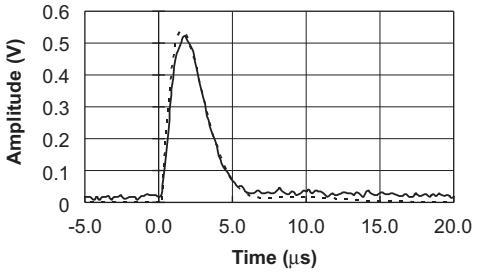

Fig. 3. Simulated (dashed) and measured (solid) responses of the shaper. The measured data are from the 5.8 MeV α-particle from ^{249}Cf and the simulation is for the corresponding number of e^-'s (1.6×10^6).

As a Gaussian-shaped step response provides favorable SNR characteristics, the shaper has a Gaussian-shaped band pass characteristics [5,6]. The simulated and measured shaper responses agree closely and are shown in Fig. 3.

In testing an earlier prototype, it was found that the $1/f$ noise at the shaper output significantly contributed to the noise in the energy branch. To lessen this contribution, a second filter was added at the output of the first shaper. The transient response of the shaper with this additional filter is shown in Fig. 4. The output of the filter is a bipolar pulse. The signal peak is inverted because the signal from

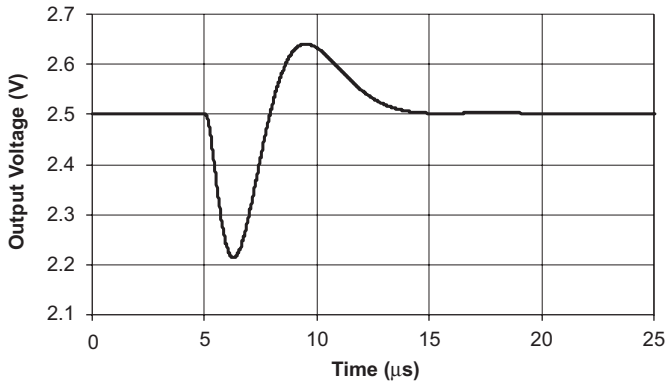

Fig. 4. Simulated response of a shaper with bandpass filter. The bandpass filter was added when an earlier prototype revealed $1/f$ noise greater than predicted by vendor supplied simulation models.

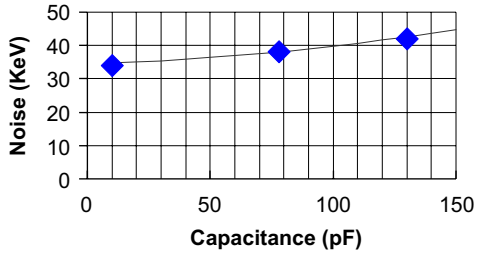

Fig. 5. Simulated (line) and measured (diamond) resolution (FWHM) performance of the energy branch. These measured values are with ideal capacitors.

the shaper is passed through an inverting gain amplifier to correct for the amplitude loss in the shaper. The core amplifier used was a folded cascode with a rail-to-rail class AB output stage [7,8]. The output of this added filter is not externally observable. Recognizing the importance of being able to observe this signal, revisions of HINP16C will make this signal available on an external pin.

3.3. Peak-sampling circuit

The peak-sampling circuit amplifies the signal from the pulse shaper and detects the peak of the amplified signal for both the positive and the negative pulses. The output of the peak sampler is a measure of the energy of the impacting particle. The peak sampler consists of a positive peak detector, negative peak detector, and a multiplexer. The multiplexer selects between the outputs from the positive or the negative peak detector depending on the input to the system. The positive and the negative peak detectors accept their input from the gain amplifier, track the peak, and hold the value [9].

The simulated and measured noise performance displayed as the FWHM in keV for silicon for the energy branch (consisting of the CSA, shaper and the peak sampler) is shown in Fig. 5. Data taken, using a pulser, with the IC agrees well with the simulated performance. With a capacitance at the input of 75 pF, the resolution is 38 keV. Our initial estimate of 30 keV, with 75 pF, was overly optimisitic as we used the models provided by the foundry which under estimated the $1/f$ noise. Fortunately, other researchers [18] have measured the $1/f$ noise associated with devices fabricated in the AMI 0.5 micron process. Once the parameters presented in [17,18] were inserted into the simulation, the simulated and measured responses agreed well.

3.4. Constant fraction discriminator

To generate a logic signal that reports the arrival time of a particle at the detector, a discriminator is used [10]. The output of the CSA has amplitude variations of 5000:1 and a rise time of around 80 ns. A simple leading-edge discriminator alone cannot be used in this application since a signal with 80 ns rise time would generate a walk of tens of nanoseconds. As our design goal is to generate a timing signal with no more than ± 0.5 ns walk over the usable dynamic range, a constant-fraction-discriminator (CFD) is used [11,12].

The CFD uses an analog memory element to convert the unipolar signal into a bipolar signal. Timing is done on the zero-crossing of the bipolar signal since the zero-crossing does not move in time as a function of the signal amplitude for inputs that vary only in amplitude. The zero-crossing comparator may go back and forth between the two power supply rails due to noise. A leading-edge discriminator is used to enable the zero-cross discriminator. Thus, the leading edge discriminator indicates a valid event while the zero-cross discriminator provides the time [13,14]. To ensure correct operation of the CFD, the leading-edge comparator must fire before the zero-crossing comparator does.

The CFD was driven in simulations with exponential pulses of amplitude from 1 mV to 1 V. Over this range, corresponding to 17,000 to 17×10^6 e s, the simulated walk was less than 500 ps. See solid line in Fig. 6. The absolute delay of the CFD circuit is approximately 50 ns.

Experimental data from three different channels are shown as symbols in Fig. 6. The absolute delay is removed by normalization to the delay measured with 20 MeV at the input. The channel-to-channel variations are small (less than 500 ps) for inputs greater than 2 MeV. Furthermore, the agreement between measured and simulated responses is, for the most part, quite good. Variation between channels occurs for inputs less than 2 MeV and a difference between the simulations and the data exists for energies greater than 20 MeV. The channel-to-channel variation is likely caused by an inability of the zero-crossing circuit to dynamically null its internal offsets to a sufficiently low-level while the latter disagreement is likely an earlier than predicted transition to leading-edge mode (occurs when the zero-crossing comparator fires before the leading-edge comparator).

Finally, with an input level of 5 MeV, the simulated time resolution (jitter) was 1 ns. This agrees very well with the

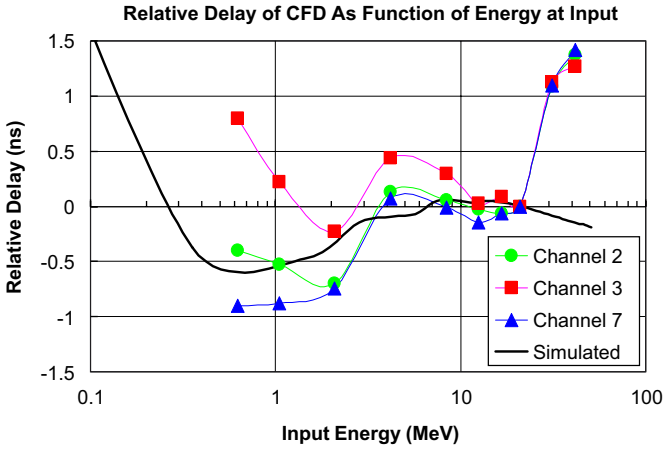

Fig. 6. Walk performance of CFD circuit. Both simulated and measured responses are shown. Measurements were made on three channels (2, 3, 7) on a single chip.

measured time resolution for α-particles of 5.8 MeV which was also 1.0 ns when the IC was used with external preamplifiers.

3.4.1. Digital-to-analog converter

The digital-to-analog converter (DAC) is used to correct offsets associated with the leading-edge detector. It consists of a binary weighted array (weights: 1, 2, 4, 8, 16) of current sources and current sinks. The most significant bit indicates the algebraic sign and whether the current sources or current sinks are used. In other words, the data format is sign/magnitude with five bits of magnitude in both the positive and the negative direction.

An output voltage is created by either sourcing or sinking current through a 0.5 kΩ resistor, connected to analog ground (AGND = 2.5 VDC). A maximum positive output voltage of 19.8 mV with respect to AGND can be achieved. The most negative output is −19.8 mV (relative to AGND). The step size is approximately 0.625 mV. Settling time (better than 1%) on the DAC outputs is 1 μs. The step size of 0.625 mV corresponds to roughly 12,000 electrons at the input to the CSA (in the high-gain mode). Offsets associated with the leading-edge discriminator are predicted to be 10 mV (3σ). This implies maximum threshold levels of 120,000 electrons.

3.5. Analog reset logic

Automatic reset circuitry has been incorporated into each channel. As discussed earlier, when a channel is hit, the channel's CFD creates a positive-going pulse (generated by a one-shot circuit with a fixed pulse width) that lasts for approximately 100 ns. This pulse is then used to trigger a second one-shot. This second monostable produces a negative-going pulse with a variable pulse width. The delay, common to all channels on the IC, can be varied by controlling an external voltage. Fig. 7 illustrates that the delay can be reliably varied from a few hundred

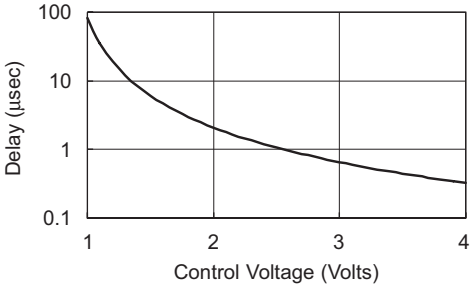

Fig. 7. Variable one-shot delay time versus control voltage. Delays ranging from around 300 ns to 10 μs are easily achievable by adjusting an external control voltage.

nano-seconds to around 100 μs by varying the control voltage between 1 and 4 V. A control voltage of 2.5 V yields a delay of 1 μs which is approximately equal to the peaking time of the shaper.

3.6. Time-to-voltage converter

The time of any channel relative to an external reference is measured using a time-to-voltage converter (TVC). These converters (one per channel) are started by the individual CFD's and stopped by the external reference. The reference is the result of an external logic decision, which can include the chip "ORs".

The TVC is designed to operate in two different settings, 250 ns/V and 1 μs/V. The TVC can be switched between these two modes by changing the value of a bit in the configuration register. The measurement is stored as an analog voltage across a capacitor [15]. The output stage of the TVC is a source follower which buffers the voltage across the capacitor. The voltage across the capacitor is proportional to the time that the channel was hit relative to a common stop signal.

3.7. Common circuits

In addition to the 16 processing channels, there exists a 17th channel running down the center of the IC. This additional channel contains the common bias and digital circuits. The bias circuitry consists of a bandgap voltage reference and related current references. The bandgap voltage reference produces a stable voltage (1.23 V) with respect to both power supply and temperature variations. This reference voltage and its associated PTAT current source, generated in the common (central) channel, are used to bias the majority of the circuits on the IC.

The TVC, however, requires a temperature-independent constant current to charge a capacitor, thereby, producing a voltage that varies linearly with time but with little dependence on both temperature and supply voltage. The current used by the TVC is generated by a constant-current source derived from the bandgap reference. A resistor, with an approximately zero temperature coefficient, sets the value of the charging current (different for the two TVC

ranges). The zero temperature coefficient is achieved by using two differently doped poly layers, one possessing a negative temperature coefficient while the other a positive one.

The common digital block consists of circuits that can report the current status of the channels in the IC and a configuration register. The configuration register is loaded with bits to select the features that the IC possesses.

4. Area and power distribution

Fig. 8 shows the distribution in the area occupied by the individual blocks in the chip. Fig. 9 shows the total power distribution among different blocks in the IC. The total current consumption for all 16 channels and the common channel is approximately 160 mA. Under normal conditions, the IC operates at 5 V dissipating a total power of 800 mW or 50 mW/ch.

5. ASIC layout

The layout of HINP16C (Fig. 10) has the following features (Table 1):

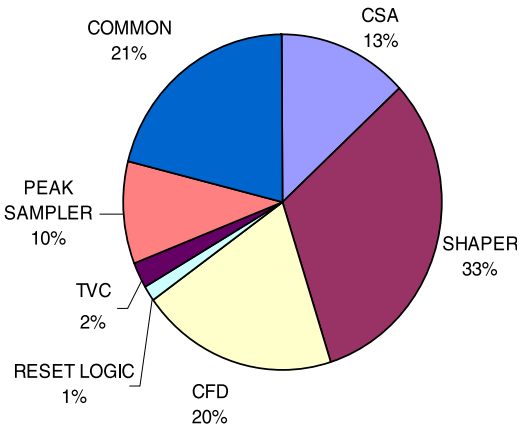

Fig. 8. Area chart.

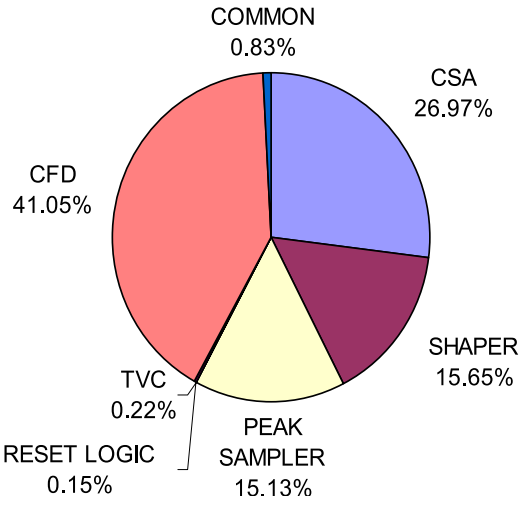

Fig. 9. Power chart.

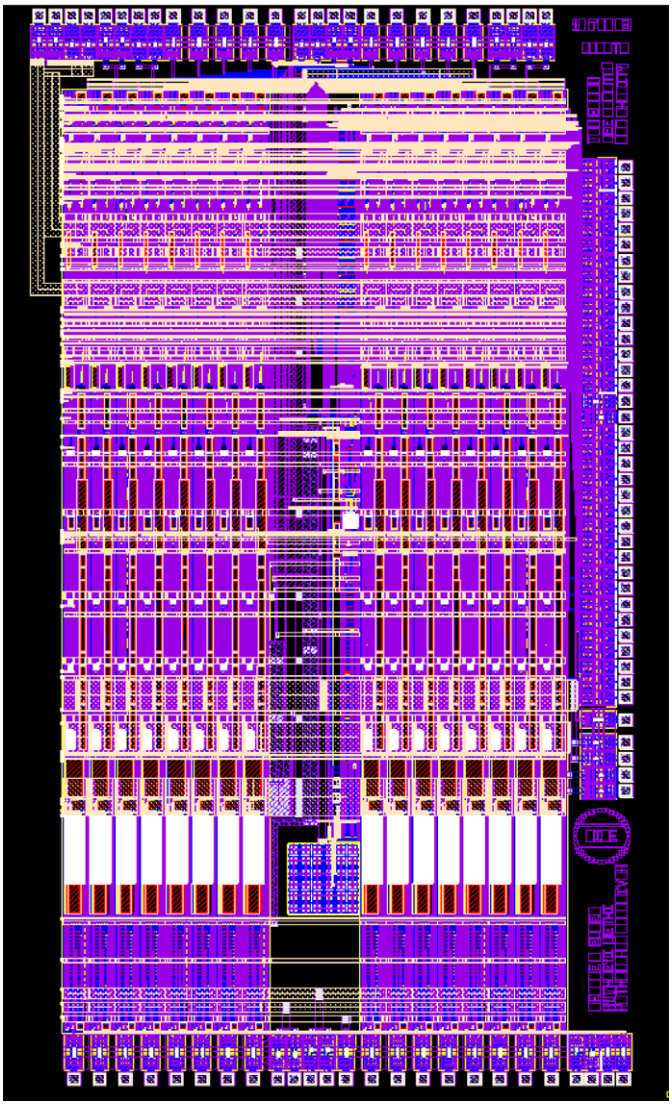

Fig. 10. HINP16C layout. The biasing and circuits used for configuring the IC as well as for readout are located in the center ("common" channel) of the chip. Eight channels lie to the left of this "common" area, and eight channels lie to the right.

Table 1
Measured performance

Parameters	Value (measured)
Energy branch	
Resolution at 75 pF	38 keV
Linear range in LOW gain mode	500 MeV
Linear range in HIGH gain mode	100 MeV
CSA gain in LOW gain mode	3 mV/MeV (0.08 mV/fC)
CSA gain in HIGH gain mode	15 mV/Mev (0.4 mV/fC)
Timing branch	
Walk through CFD	<1 ns over a range of 40 dB
Jitter	1 ns

- The chip width is 3.54 mm, and the height is 6.43 mm.
- To minimize cross-talk between channels, each channel is surrounded by a guard ring which is ultimately

connected to the substrate. The substrate line is connected to a separate pad, isolated from the voltage supply lines.
- Sensitive analog circuits within a single channel are surrounded by guard rings which helps isolate them from other circuits within the channel.
- To minimize cross-talk between analog and digital signals, the analog and digital lines were shielded by running a metal line (GND) between them.
- Physical distance was also used to isolate sensitive analog circuits from possible sources of crosstalk.

6. HINP16C performance

Tests were performed with both the internal and two external CSAs on both the linear and timing functions. One of the external CSAs had about the same gain (12 mV/MeV) as the high-gain internal CSA and the other external CSA has a gain about 4 times greater [16]. In addition to pulser tests, we tested with both α-particles and conversion e^-'s.

Our α-particle tests used a ^{249}Cf source for which the prominent α-decay branch (80%) feeds an excited state which γ-decays to the ground state (with a mean live time $\tau = 0.65$ ns or $t_{1/2} = 0.45$ ns) via the emission of a 388 keV γ-ray. The α–γ coincidence allowed us to test the timing resolution of the system. The 388 keV γ-ray was detected with a cylindrical CsF scintillator of diameter 24.5 and 40 mm long. The time resolution (FWHM) of the CsF (to this photon) using a CFD is approximately 0.25 ns. The Si used for the α-particle tests is 300 μm and 18 pf when depleted. The cables added another 20 pf.

A ^{207}Bi source, with a highly converted 1063 keV transition, is used to provide e^-'s of 975 and 1047 keV. The Si used for detecting e^-'s was 1.5 mm thick, and 50 pf when depleted (it is a very large single area device, 25.4 mm × 25.4 mm). Again cables added another 20 pf.

The pulser tests verified the simulated signal shape and gain of the internal CSAs and shaper, see Fig. 3. The full dynamic range was also verified, and even a larger range could be used if non-linearities can be tolerated or corrected for. (The non-linearities for both polarities were designed to be compressive.)

Pulser resolution tests (diamonds in Fig. 5) indicated that the noise slope is consistent with the simulated performance. The FWHM noise values with (ideal) capacitors of 11, 78 and 130 pf are 34, 38 and 42 keV, respectively. This should be compared to the simulated values of 35, 38 and 43 keV, respectively.

Figs. 11 and 12 show the results of our tests for the α–γ tests with the external (50 mV/MeV) and internal (high-gain) CSAs, while Fig. 13 shows the conversion e^- test with the high-gain external CSA. (The results for the 12 mV/MeV external CSA are not shown but the results are included in Table 2.)

The source tests with the external CSA yielded 18 and 28 keV resolution (FWHM) for e^- and α-particles,

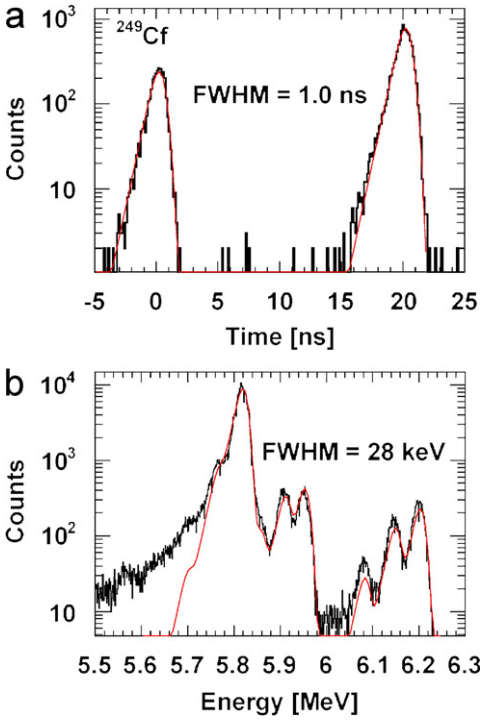

Fig. 11. (a) Time and (b) energy spectra of a ^{249}Cf source obtained using an external high gain (50 mV/Mev) CSA. The time spectrum presents two measurements of start-stop time difference offset by 20 ns. The lifetime of the $t_{1/2} = 0.45$ ns intermediate state is easily observed. Advancing time runs to the left. For reference the upper two energy peaks seen in (b) are separated by 54 keV. The resolutions are extracted from the fits (lines) which are (a) an exponential convoluted with a Gaussian resolution function and (b) slightly skewed Gaussians with the known relative intensities.

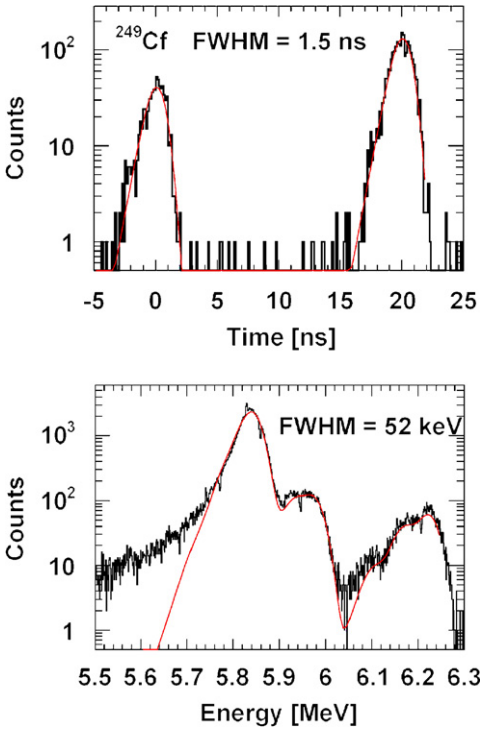

Fig. 12. Same as Fig. 11 except using the internal high-gain (15 mV/MeV) CSA.

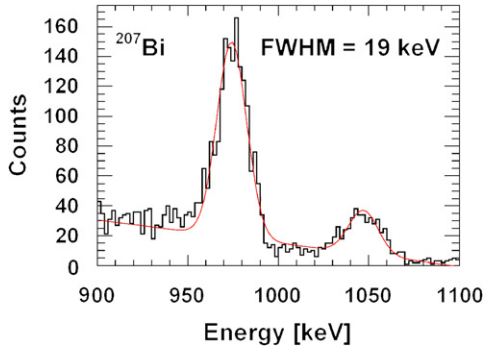

Fig. 13. The energy spectrum from a ^{207}Bi source using an external high gain (50 mV/MeV) CSA. The Si had a rather large capacitance and neither it nor the CSA were cooled. The full range of the system configured for this test was 35 MeV.

Table 2
Source tests (FWHM)

Test	E_{res} (keV)	T_{res} (ns)
e^-, ext. 50 mV/MeV	18	
α's, ext. 5 mV/MeV	27	1.0
α's, ext. 12 mV/MeV	38	1.0
α's, int. 15 mv/MeV	52	1.5

respectively. The time resolution for α-particles of 5.8 MeV in this mode is 1.0 ns (the correction for the contribution from the γ-ray stop is negligible). The linear range with this external CSA is about 35 MeV. With an external CSA of a gain similar to that of the high-gain internal CSA, the α-particle energy resolution was 38 keV.

The energy and time resolution using the high-gain internal CSA (15 mV/MeV) are 52 keV and 1.5 ns, respectively. Assuming that the high-gain external CSA measurement provides a measure of the intrinsic resolution limit resulting from charge recombination and dead layers in the Si itself, the electronic resolution of in internal CSA is 44 keV. This value is somewhat larger than expected based on the pulser study for which at a similar capacitive load (approximately 40 pf) 36 keV was achieved. This indicates that the actual detector system cannot be accurately modeled as a single ideal capacitor.

Finally, the fact that the external CSA of approximately the same gain as the internal CSA produced superior resolution (38 keV as compared to 52 keV), indicates that the resolution when using the internal CSA is completely determined by the CSA. (The shaper and peak sensor make negligible contributions.)

The current version of the IC displays a large temperature sensitivity. For some time the origin of this sensitivity was unknown. After careful investigation of this problem, it was discovered that as a result of an oversight while doing the layout of the chip, the signal grounds for the energy and timing branches of the IC were tied together. While there should be no currents flowing in the signal ground for the energy branch, this is not the case. The return currents for the DACs in the CFD circuits have some temperature dependence and consequently the analog ground reference for the energy output displays the same temperature dependence. In a revision of the IC scheduled for fabrication in the near future, the energy and timing signal return paths share no common impedance and the sensitivity to temperature will be greatly improved.

7. Summary

A CMOS chip has been designed, fabricated, tested and used in experiments. The present paper details the chip functionality and the results of pulser and source tests. The resolution achieved with the present chip is sufficient for most of the experiments in the HiRA program. Five experiments have already been performed. Furthermore, the flexibility offered by this chip (various triggering and readout modes as well as the external CSA option) makes it suitable for use in many mid-sized Si arrays in use or planned for low-energy nuclear physics. Presently, arrangements are being made to use it with other midsized arrays.

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