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Multi-electrode CZT detector packaging using polymer flip chip bonding

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Abstract

Polymer flip chip bonding has been used to package a multi-electrode CZT detector. During the packaging process the temperature of all components was kept less than 80°C. The size of the conductive epoxy eontacts is less than 120 μm in diameter. Thermal cycling, and random and structural vibration tests indicate reliable detector–substrate interconnection and rugged construction. © 2001 Elsevier Science B.V. All rights reserved.

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1. Introduction

The packaging of multi-electrode room-temperature detectors has become an important issue considering the desire for compact packages, the limitations due to the material properties and the small size of the contacts. One difficulty arises from the requirement to keep the temperature of the detector crystal below a certain limit. For CZT detectors, for example, this limit is below 150°C [1].

Two common methods are used to interconnect electronic components – wire bonding and flip chip assembly. The main differences between the two techniques are the way the components are placed and the means of interconnection. The components for wire bonding are placed with their contact pads facing in the same direction, whereas in the flip chip process the components are mounted with their contact pads facing each other. Wire bonding uses a thin wire to connect the pads of the components while flip chip interconnection is achieved by placing a conductive metal bump between the pads of the components. High-density packaging is normally achieved by using flip chip technology.

Both interconnection techniques have been used to package multi-electrode radiation detectors. The wire bonding technique, with some modifications, has been adapted to interconnect CZT strip detectors for space applications [2]. Flip chip assembly using Indium solder bumps has been successfully used to interconnect a pixel CZT detector to a silicon substrate [3]. This paper describes an

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alternative, low-temperature flip chip bonding technique applied to the packaging of a multi-electrode CZT detector.

2. Polymer flip chip bonding

The polymer flip chip (PFC) bonding technique utilizes silver-filled conductive epoxy to electrically connect the contacts of electronic components [4–6]. Polymer bumps are stencil printed and can be cured at temperatures as low as room temperature. The stencil printing process enables conductive flip chip bumps to be printed in fairly small geometries. Minimum aperture sizes down to 50–60 μm are presently feasible enabling conductive bumps to be printed at 125 μm pitch centers. Fig. 1 illustrates the basic steps of the polymer flip chip bonding process. The drawings depicted in Fig. 1 are for illustrative purposes only and are not drawn to scale.

Step 1: This drawing illustrates the separate components to be assembled. The top (thicker) component is the CZT detector chip that will be flipped and bonded to the substrate – the bottom (thinner) low-temperature cofired ceramic (LTCC) substrate. Gold metallized contacts are depicted on the top surface of the CZT detector. The detector gold contact array is intended to mate with an array of thick film, gold metallized pads on the LTCC substrate. Both components are cleaned and inspected before proceeding to the bonding process.

Step 2: At the beginning of the polymer bonding process, small conductive bumps are stencil printed onto the CZT detector using conventional screen printing equipment and techniques. Illustrated is a thin stainless steel stencil with small (e.g. 100 μm) aperture openings aligned over the CZT contact pad array. Silver-filled conductive epoxy ink is squeezed through the aperture openings and deposited onto the anode pixel pads forming the flip chip bumps.

Step 3: The CZT detector is then placed into a circulating oven (e.g. 70°C, 4–5 h), to cure the polymer bumps. Bump height following curing typically ranges from 35 to 45 μm, depending on a number of factors such as the type and viscosity of the conductive ink, the stencil thickness and printing parameters. Uniformity of bump height, however, is fairly consistent (± 2 μm) across individual components.

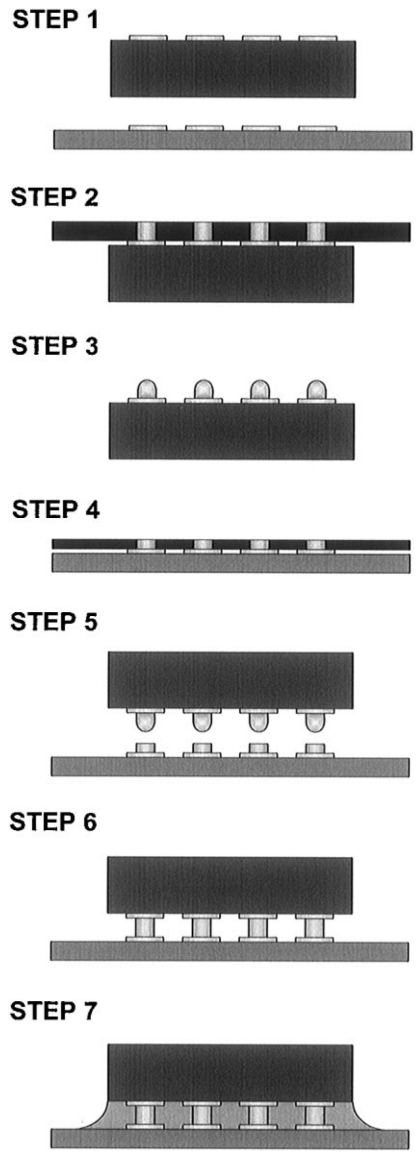

Fig. 1. Polymer flip chip bonding process.

Step 4: A stencil with apertures arrayed in a mirror image of those on the CZT detector is then used to deposit epoxy bumps onto the LTCC substrate. These bumps are preferably 15–25 μm larger in diameter than the bumps stenciled onto the CZT detector. The stenciling process and materials are otherwise identical to Step 2.

Step 5: The stenciled bumps on the LTCC substrate are left in a wet state until the detector bumps are aligned and pressed into them. The cured bumps on the CZT detector provide a coplanar standoff for preventing excessive spreading of the wet epoxy when the components are pressed together.

Step 6: Placement accuracy of the CZT detector onto the LTCC substrate typically varies from 5 to 25 μm, depending on the type of equipment used. Once assembled, the components are placed into the oven again and cured as in Step 3.

Step 7: Due to the low shear strength of the small epoxy bumps, long-term reliable interconnect requires that the entire underside of the CZT detector be epoxy bonded to the LTCC substrate. This process step, called "underfilling", involves the dispensing of a low-viscosity, non-conductive epoxy around the edges of the detector which is then wicked between the surfaces by capillary action. Once again the components are placed into an oven and cured for approximately 1–2 h.

The conductive polymer flip chip assembly offers several advantages compared with conventional solder reflow flip chip technology. The conductive inks are easily stenciled onto the surfaces of the materials to be assembled, eliminating either electroplating or thin film vacuum deposition of solder. The simplicity of this manufacturing process, therefore, results in lower assembly costs. Yet, the performance characteristics, in terms of interconnect density and reliability, are very competitive with solder flip chip.

Of particular importance to CZT detector packaging are the low processing temperatures enabled by polymer flip chip assembly. Most conductive inks are cured at temperatures between 120°C and 150°C, well below the melting point for eutectic solder at 182°C and typical peak processing temperatures of 210–240°C. The ink used on this project (EPO-TEK E4110-PFC) is a two-component, silver-filled, conductive epoxy system that can be cured at room temperature, if necessary, and still retains reasonably good volume resistivity (0.005 Ω cm).

Table 1
Epoxy curing schedule

E4110-PFC	U-300
Room temp. = 72 h	Room temp. = 8 h
60°C = 6 h	60°C = 3 h
80°C = 3 h	80°C = 1 h
100°C = 1 h	100°C = 20 min
150°C = 15 min	150°C = 3 min

Table 2
Epoxy properties

E4110-PFC	U-300
Mixing ratio: 10 part A to 1 part B	Mixing ratio: 10 part A to 1 part B
Volume resistivity: $< 0.005\,\Omega\,\mathrm{cm}$	Volume resistivity: $1 \times 10^{14}\,\Omega\,\mathrm{cm}$
CTE: 60×10^{-6} m/m/K	CTE: 32×10^{-6} m/m/K
T_g: subambient/flexible	T_g: 130°C
Operating temp.: continuous 150°C	Dielectric constant: 4.1

An important step in the assembly process is the dispensing of the non-conductive epoxy between the mated surfaces. For this "underfilling" process, a two-component epoxy material (EPO-TEK U-300) was chosen for its adhesive and low-viscosity characteristics, enabling the epoxy to be readily drawn under the CZT by capillary action.

Table 1 shows the curing schedule of the epoxy materials used in this work and Table 2 lists some of their properties. Lowest contact resistance is achieved if the metal surfaces to be joined are plated or deposited with a noble metal such as palladium or gold.

An important property of the polymer bumps is their ability to withstand thermal shock and thermal cycling without braking the contact [4]. This is due to the elasticity of the bumps that can absorb stress without cracking when there is a coefficient of thermal expansion (CTE) mismatch between the assembly components. This feature is important in applications, such as space instruments, where the detector assemblies could be exposed to wide temperature variations.

3. CZT detector assembly

The PFC technique was used to package an imaging CZT detector with orthogonal coplanar electrodes [7,8]. The CZT detector is a single-crystal 5 mm thick slab with a continuos gold contact on one side and pixel-strip gold pattern on the other side [7]. The electrode surfaces are square with dimensions of 12×12 mm. All contacts are made using thin film gold metallurgy. The patterned side of the detector was attached to a mating pattern on the LTCC substrate.

LTCC technology was selected for fabricating the mating substrate with the primary motivation to minimize interference between the detector electrodes and the interconnecting circuit traces deposited on the substrate. In addition, the PFC process requires flat mating contact pads. LTCC technology permits fabrication of flat contact pads that fully cover the vias with no circuit trace that extends beyond their boundaries.

Fig. 2 depicts the mating patterns on the detector side and the LTCC mounting surface. The CZT detector is patterned with 64 pixel electrodes and long strip electrodes surrounded with a guard electrode. The CZT pixel pads are 200 μm in diameter and are placed on a 1 mm grid. Three circular voids in the guard electrode are used as fiducial alignment marks. The LTCC surface has an electrode pattern with 180 μm diameter pixel pads and fiducial marks that are the mirror images of the corresponding CZT detector patterns. The guard electrode is attached through four contact pads placed around the pixel contact area of the LTCC pattern. An additional row of contacts, similar to the pixel contacts, is used to connect to the detector strip electrodes. An additional contact pad is placed near one of the corners of the LTCC substrate. This pad is used to attach a wire to the side of the detector with a continuos electrode (cathode) providing a bias voltage to the detector.

The contacts on the surface of the LTCC represent the ends of filled vias. The diameter of the filled vias and flat contact pads on the substrates is 180 μm. The vias pass through the full 1.25 mm thickness of the LTCC substrate. This separates the interconnecting circuit traces from the field region near the CZT anode surface. Fig. 3 shows a cross-section example of a filled via (top drawing, not to

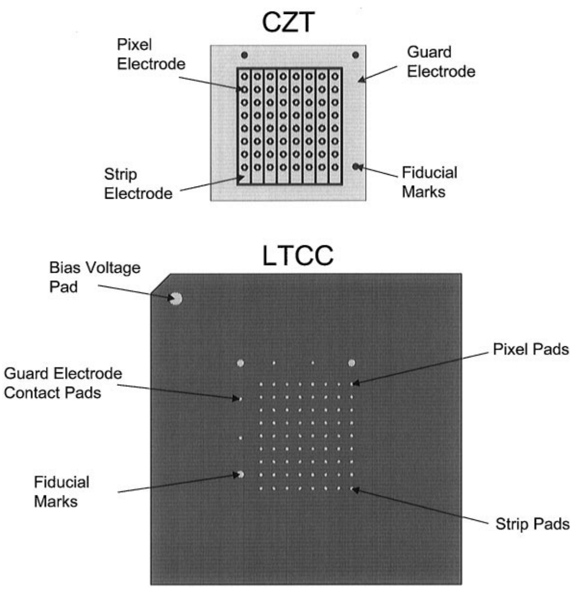

Fig. 2. Contact patterns of CZT detector (top) and LTCC substrate (bottom).

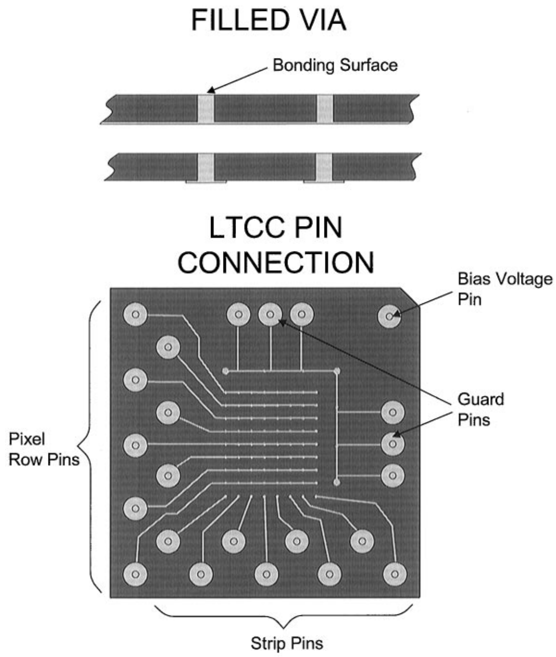

Fig. 3. Example of filled via (top) and LTCC interconnection pattern.

scale) and the contact pattern on the bottom side (opposite to the CZT detector) of the LTCC.

The signals from the detector through the filled vias and interconnecting traces are brought to brazed pins on the bottom of the substrate. The detector pixels from each pixel row perpendicular to the strips are connected together (eight per row). Each pixel row is connected to a pin. The strips are connected each to a separate pin. The guard electrode is connected to six pins that are added for mechanical strength. A pin in the corner of the LTCC is used to supply bias voltage to the bias electrode pad on the opposite side of the LTCC.

The CZT detector is very brittle and easily chipped if not properly handled and the LTCC substrate has brazed pins on the bottom, which can be bent or broken. Consequently, for this project we designed a steel plate for protecting and holding both components during the stencil printing process. Cavities were machined into the plate for nesting the CZT and LTCC components such that their surfaces were positioned approximately 180 μm above the plate's surface. Vacuum holes placed directly underneath the components held the parts from shifting during the stencil operation. Using the steps described in the previous section the CZT detector was attached to the LTCC substrate. The aperture size used for printing bumps on both the CZT and LTCC components was 100 μm diameter, resulting in a finished bump diameter between 115 and 120 μm and bump height ranging from 20 to 22 μm. After the bumps were printed and cured in the oven scanning electron microscope (SEM) pictures were taken of the bumps.

Three SEM pictures are shown in Fig. 4. The first picture shows a section of the detector surface with the pixel pattern. The polymer bumps (darker circles) are well aligned which is crucial for achieving reliable interconnection. The second picture depicts a single bump at higher magnification. The diameter of the bump is in good agreement with the aperture opening of the ink-printing stencil. The third picture was taken after tilting the sample 75°. From this picture the height of the bump can be estimated – slightly higher than 20 μm. The SEM inspection of the bumps along with some additional optical tests indicates that all polymer

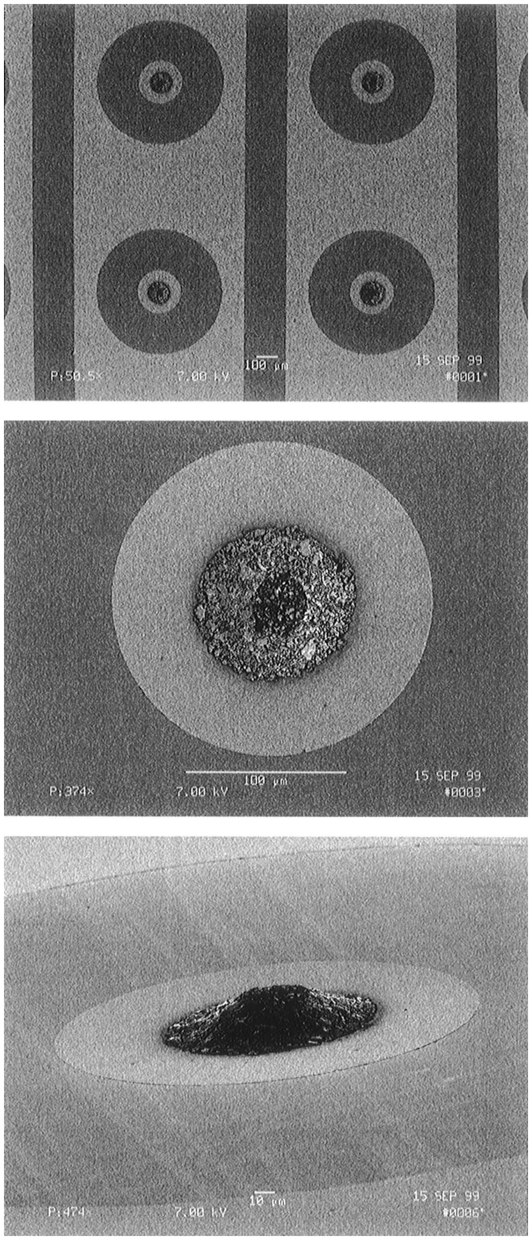

Fig. 4. SEM pictures of cured polymer bumps.

bumps have uniform size with very good placement registration.

Once the epoxy bumps on the CZT detector were cured and the LTCC substrate bumps were printed, the components were ready for assembly. Precision alignment and placement equipment was then used

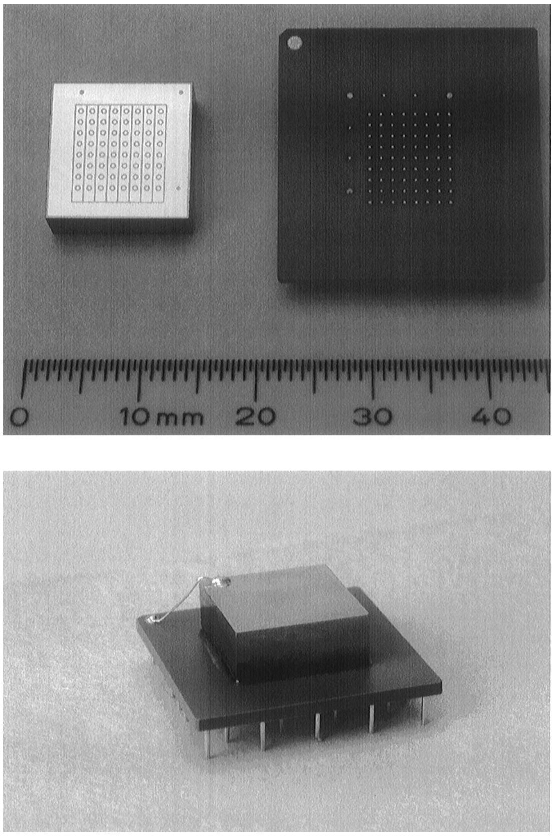

Fig. 5. CZT detector and LTCC substrate before and after the PFC assembly process.

for attaching the parts together. A vacuum tip held the CZT detector while a look-up camera was used to align the detector bumps with respect to the bumps located on the LTCC substrate. The detector was then lowered onto the substrate and pressed into the wet epoxy bumps with sufficient force to bring the cured bumps into contact with the surface of the substrate pads, causing the wet epoxy to envelop the cured bumps. The joined parts were then placed in a circulating oven at 70°C for 6–7 h to cure the substrate epoxy.

After the contacts have been cured the detector assembly was underfilled with low viscosity epoxy. This epoxy was then cured at 70°C for 2 h. The final step in assembly was to connect a thin wire, using conductive epoxy, between the top cathode surface of the CZT detector and its biasing pad on the surface of the LTCC substrate. Fig. 5 depicts the assembly parts before and after the PFC bonding process.

4. Detector characterization

CZT strip detectors and their fabrication are under study at the University of New Hampshire's Space Science Center under NASA's High Energy Astrophysics Supporting Research and Technology Program. The goal of these studies is the development of large area arrays of closely packed imaging CZT spectrometer modules to be used in hard X-ray and gamma-ray telescopes [9, 10] which can be deployed on either high-altitude balloons or space craft.

Using PFC technology four identical detector assemblies have been built. The initial detector performance characterization has been presented elsewhere [11]. We used one of the assemblies to perform tests in environments appropriate to the space applications. Addressing the reliability issues is an important part of these studies.

The feasibility in these applications of the electrical and mechanical PFC bonding technique presented here has been demonstrated in thermal cycle and vibration tests. The test detector assembly was cycled in the temperature range $-20°C$ to $+50°C$ at a rate of 20°C/h. It was then exposed to random and structural vibration in the thrust and lateral axes according to qualification levels appropriate for an instrument launched on a Delta II vehicle. Leakage current measurements on all pixel and strip channels were performed before and after these environmental exposures and demonstrated no significant change.

5. Conclusion

The PFC technology was used to package a CZT imaging detector. During all technology procedures the assembly components were kept at temperature under 80°C. A methodology to bond large parts such as the CZT detector has been developed. The assembly process is relatively straightforward and should be capable of allowing large arrays of detectors to be mounted on a single substrate. The

PFC method can be used to attach detectors directly to silicon substrates for compact detector-electronics assemblies. The initial environmental tests indicate good reliability of the assembly for meeting the standards established for space instrumentation. However, in order to build reliability confidence and to estimate the failure rate additional tests need to be performed.

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