A High Density Low Cost Digital Signal Processing Module for Large Scale Radiation Detectors

Hui Tan, Wolfgang Hennig, Mark D. Walby, Dimitry Breus, Jackson T. Harris, Peter M. Grudberg, William K. Warburton

***Abstract*—A 32-channel digital spectrometer PIXIE-32 is being developed for nuclear physics or other radiation detection applications requiring digital signal processing with large number of channels at relatively low cost. A single PIXIE-32 provides spectrometry and waveform acquisition for 32 input signals per module whereas multiple modules can be combined into larger systems. It is based on the PCI Express standard which allows data transfer rates to the host computer of up to 800MB/s. Each of the 32 channels in a PIXIE-32 module accepts signals directly from a detector preamplifier or photomultiplier. Digitally controlled offsets can be individually adjusted for each channel. Signals are digitized in 12-bit, 50 MHz multi-channel ADCs. Triggering, pile-up inspection and filtering of the data stream are performed in real time, and pulse heights and other event data are calculated on an event-by event basis. The hardware architecture, internal and external triggering features, and the spectrometry and waveform acquisition capability of the PIXIE-32 as well as its capability to distribute clock and triggers among multiple modules, are presented.**

***Index Terms*—Gamma-ray Spectrometer, Multi-channel ADC, Detector Arrays**

I. Introduction

LARGE scale radiation detectors have been increasingly used by nuclear scientists around the world to conduct experiments in areas such as nuclear science, nuclear astrophysics, and nuclear theory to gain better understanding of the forces that bind together the basic building blocks of the universe and to make exciting discoveries of rare isotope science. To support the operations of those large scale detectors, development of new generations of readout electronics is in great demand. This is because existing off-the-shelf readout electronics is prohibitively expensive for large detector arrays, which require high density readout electronics with good timing and energy resolution that at the same time offer lower cost per channel, compared to existing solutions.

Recent improvements in the design and manufacturing of commercial analog to digital converters (ADCs) have resulted in a variety of multi-channel ADCs that are natural choice for designing such high density readout modules. We have demonstrated previously that some of those ADCs can achieve excellent energy resolution, 2.66% FWHM at 662 keV with a $LaBr_3$ or 1.78 keV FWHM at 1332.5 keV with a high purity germanium (HPGe) detector, and sub-nanosecond timing resolution with $LaBr_3$ [1]. Therefore, it is feasible to develop high density low cost readout electronics utilizing those multi-channel ADCs.

We present here a 32-channel digital gamma-ray spectrometer, PIXIE-32, which provides spectrometry and waveform acquisition for 32 input signals per module. With an optional mezzanine board that can be attached to the PIXIE-32 main board to accept another set of 32 input signals, a total of 64 input signals can be processed by a combined PIXIE-32 main and mezzanine board (PIXIE-32×2), thus further increasing the board density and reducing the cost per channel. The hardware architecture, internal and external triggering features, and the spectrometry and waveform acquisition capability of the PIXIE-32 as well as its capability to distribute clock and triggers among multiple modules, are discussed.

II. Hardware Development

A. System Block Diagram

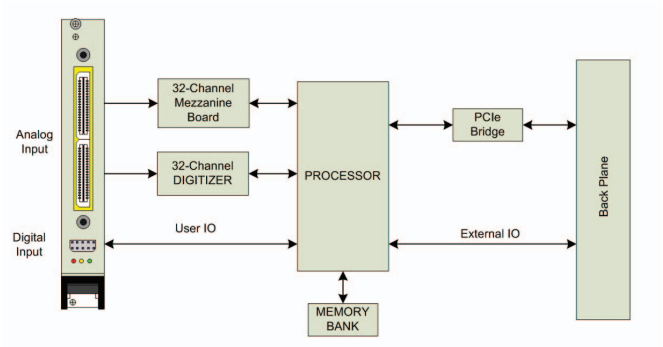

Fig. 1. System diagram of the PIXIE-32.

The system diagram of the PIXIE-32 is shown in Fig. 1. The PIXIE-32 is a 3U PXI Express (PXIe) card housed in a PXIe chassis. On the front panel of the PIXIE-32 is a high density connector, which can accept up to 64 single-ended analog signal inputs. 32 of such signals will be routed to the main

This material is based upon work supported by the U.S. Department of Energy under Award Number DE-SC0006318.

Hui Tan, Wolfgang Hennig, Mark D. Walby, Dimitry Breus, Jackson T. Harris, Peter M. Grudberg, and William K. Warburton are with XIA LLC, Hayward, CA 94544 USA (phone: 510-401-5760; fax: 510-401-5761; e-mail: htan@xia.com).

978-1-4799-1047-2/13/$31.00 ©2013 IEEE

board whereas the other 32 can be connected to the optional mezzanine board.

Each PIXIE-32 has a central processor (a Xilinx Artix-7 field programmable gate array (FPGA)) which handles signal processing and communications throughout the board. The processor accepts and processes data streams from the ADCs, stores processed data (histogram and list mode data) in the on-board DDR2 SDRAM, and outputs processed data to the host computer through the PCIe Bridge and Backplane. In addition, the processor can also input or output external or internal triggers through the front panel connector and backplane.

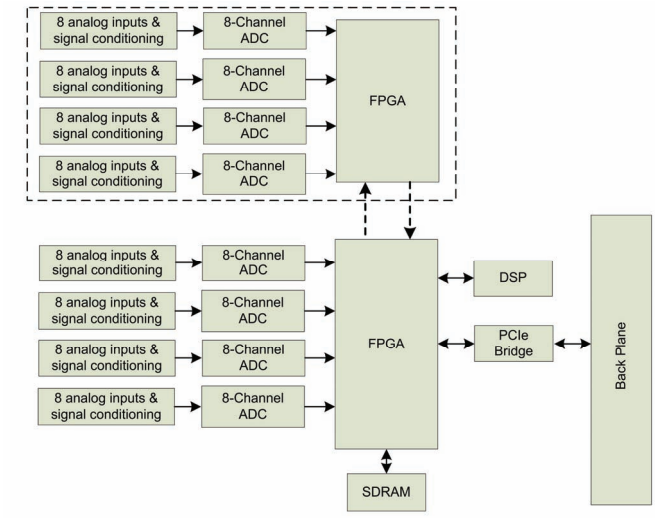

Fig. 2. Block diagram of the PIXIE-32.

A detailed block diagram of the major components of the PIXIE-32 is illustrated in Fig. 2. Shown in the dashed line box is the optional mezzanine board, which has the capability to digitize 32 analog signals through its four 8-channel ADCs and then preprocess the ADC data streams with its FPGA before send the preprocessed data to the main board FPGA for final processing.

A digital signal processor (DSP) is connected to the FPGA, providing the capabilities to configure the real time signal processing operations in the FPGA based on parameters sent by host computer software and to conduct special tasks through user supplied DSP code (e.g., custom pulse shape analysis).

B. Signal Processing

Each of the 32 channels in a PIXIE-32 can accept signals directly from a detector preamplifier or photomultiplier. Upon entering the PIXIE-32 board through the front panel high density connector, the input signals are first adjusted for voltage offsets through Digital to Analog Converters (DACs), one for each channel. Signals are then digitized by 12-bit, 50 MHz 8-channel ADCs. The ADC serial data, at the double data rate (DDR) of 300 Mb/s, are then sent to the FPGA, which first deserializes the ADC data stream and then performs triggering, pile-up inspection and filtering of the ADC data in real time. Pulse heights and other event data are calculated on an event-by event basis by the FPGA.

C. PCIe Interface

The PIXIE-32 utilizes PCIe as an interface to the host PC. The Gennum 4124 PCI-to-local bridge, which provides a ×4 PCIe interface and supports theoretical limit of 800 MByte/s per chassis slot to host PC, is used on the PIXIE-32 as the PCIe Bridge. With suitable chassis and host PC, parallel readout of multiple PIXIE-32 modules in a chassis is feasible. For instance, a host PC with ×16 PCIe slots can read four PIXIE-32 modules in parallel. The PIXIE-32 PCIe interface is also compatible with PXIe peripheral and hybrid slots.

D. Data Storage and Readout

The on-board 2 Gb DDR2 SDRAM is split into two blocks, one for storing waveform data and the other for storing MCA histograms. Each channel has a 32768-bin MCA histogram with 32-bit depth, and the histograms are accumulated in real time. The list mode data consisting of waveform data with channel identifiable event headers are first buffered in the FPGA with dual port memory (DPM) blocks. Once sufficient data are accumulated in the DPM blocks for a given channel, such data are then moved to the SDRAM in block transfer mode.

The list mode or histogram data are read out by the host PC via the PCIe interface using direct memory access (DMA) transfers. A SDRAM controller has been built in the FPGA to coordinate the access to the SDRAM by multiple processes: (1) updating the MCA histograms, (2) writing list mode data to the SDRAM, and (3) reading out list mode data to the host PC.

E. Clock and Trigger Distribution

Fig. 3 illustrates the clock distribution scheme of PIXIE-32. The primary clock source is the common 100MHz differential clock provided by the PXIe backplane.

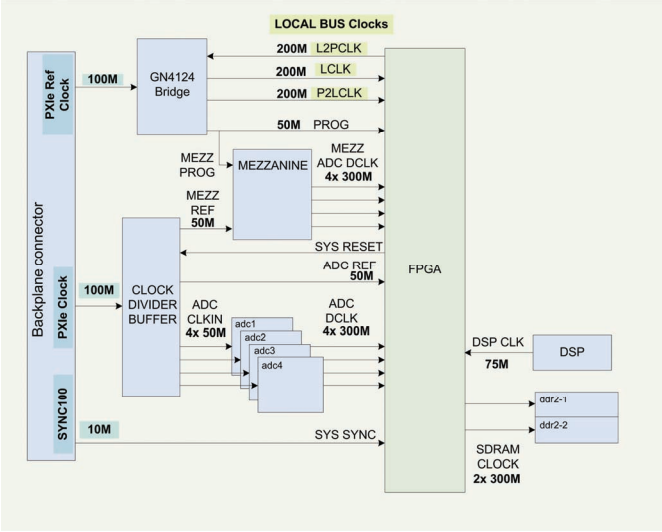

Fig. 3. Clock distribution of the PIXIE-32.

The PXIe 100MHz clock is divided and buffered by the clock divider/buffer to generate the ADC reference (low jitter) clocks at 50MHz. On power-up, the standard 10MHz PXI clock from the backplane is used to program the clock divider/buffer chip to generate all 50MHz clocks. Once

978-1-4799-1047-2/13/$31.00 ©2013 IEEE

programmed, each ADC returns a 300MHz LVDS clock to the FPGA as the ADC data clock for synchronous DDR data sampling. The clock divider/buffer is reset synchronously with the SYNC100 pulse from the backplane (10 MHz periodic) which is in phase with the 100MHz clock from the backplane. Once the FPGA is active, the FPGA drives the SYS RESET signal to synchronize the phase of the clock divider/buffer for any PIXIE-32 module that resides in the same chassis.

The PIXIE-32 has the capability to distribute triggers among multiple modules through the PXIe chassis backplane, which implements bussed and nearest neighbor lines between slots. Configurable LVTTL and LVDS lines on the PXIe backplane can be used for gate or veto, run synchronization, multiplicity information, and trigger distribution. The front panel I/O connector can be used to input or output triggers or veto/gate signals.

III. Software Development

A. PCIe Driver Development

Handel is a high-level device driver library that provides an interface to XIA's spectrometer hardware in spectroscopic units (eV, microseconds, etc.) while still allowing for safe, direct-access to the hardware. Handel's modular architecture separates the behavior of XIA's hardware from the generic behavior of the underlying communication protocol. To support the PCIe communication protocol for the PIXIE-32 hardware via the Gennum GN4124 chipset, the following tasks were completed: 1) implement basic, memory-mapped I/O via PCI Express Base Address Registers; 2) implement support for the EEPROM and Firmware Configuration Loader peripherals on the Gennum chipset; 3) research and benchmark supported DMA transfer configurations; and 4) implement one or more of the DMA configurations from 3).

The PCIe driver to support the communication from the host PC to the Gennum GN4124 chipset was developed using the driver development tool WinDriver from Jungo [2]. However, WinDriver does not currently have chip-specific support for GN4124, so all the advanced features such as interrupt handling and DMA transfers require more effort to set up. WinDriver API does provide an application that generates driver code for a specific device, as well as basic C-library code for communication with the bridge. This code only needs implementation of the hardware-specific features including definitions of the registers, interrupt handling functions, DMA engine initialization and transfer code.

B. User Interface

Commercial grade user control software that supports the operation of PIXI-32 for large number of detector channels must be user friendly, robust, and reliable. XIA is developing a new user interface (UI) framework that supports its next-generation hardware, especially high channel count systems. Of particular importance to this UI is the capability to readily adjust data acquisition parameters for potentially hundreds or thousands of channels as well as view captured waveforms or MCA histograms for that many channels.

IV. Conclusion

A high density low cost all digital spectrometer module PIXIE-32 is being developed for instrumenting large scale radiation detectors. Its relative high density (up to 64 channels in a single 3U PXIe module) and modular structure will make it suitable for processing and reading out signals from large radiation detector arrays. We will report the gamma-ray spectrometric performance of the PIXIE-32 elsewhere once the hardware is built and tested.

References

[1] H. Tan, W. Hennig, M.D. Walby, D. Breus, and J. Harris, "Evaluation of Multi-Channel ADCs for Gamma-Ray Spectroscopy", *IEEE Trans. Nucl. Sci.*, Vol. 60, Issue 2, Part 1, April 2013, pp. 599-605.

[2] WinDriver – Driver Development Tool, http://www.jungo.com/st/products/windriver/.

978-1-4799-1047-2/13/$31.00 ©2013 IEEE