A 12-Channel 14/16-Bit 100/125-MS/s Digitizer with 24-Gb/s Optical Output for AGATA/GALILEO

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Abstract-A 12-channel digitizer card with 24 Gb/s optical output and ~10 W power consumption is presented, specifically developed for the AGATA and GALILEO germanium array detectors. The card has many useful features, including: differential-input mode, end termination for both differential and common mode components of the input signals, introduction and remotely-controlled regulation of differential DC offset for dynamic range maximization, two remotely selected working ranges, built in test-pattern waveform multiplexed at the analog inputs for precise inter-channel time synchronization, optional interleaved mode for equivalent sampling-frequency multiplication, optional fast channel with remotely controlled threshold comparator working as an analog trigger for ancillary detectors. The card has been conceived for new-generation, highly-segmented, position-sensitive HPGe detectors for nuclear physics experiments, requiring digitization at 100 Ms/s 14bit or better, and is adequate for high-resolution gamma-spectroscopy and gamma-ray tracking.

I. INTRODUCTION

THE use of high-resolution flash ADC's in conjunction with I real-time digital filtering is becoming the new standard for last- and next-generation nuclear and sub-nuclear physics experiments employing segmented high-resolution semiconductor detectors [1]-[3]. The whole preamplifier signal waveforms, including their high frequency components, contain primary key information that can be used for measuring, through digital filtering techniques, important parameters like the occurrence time of the events, the time coincidences, the event energy, the three-dimensional position of the interaction points inside the detector, the angle of the trajectory of the impinging particles [4]. Availability of fast, low-power, high-resolution flash ADC's (Analog to Digital Converters), along with broad band digital-data transmission lines makes it possible to sample the entire preamplifier waveform [5]-[6], transmit it to a far receiver, and use powerful digital filters located nearby the far-end receiver for data filtering and analysis. [7]. Such architecture is nowadays a viable powerful solution alternative to using classic analog shapers with peak stretchers and slow ADC's. This 12channel digitizer card has been developed for such system architectures and more specifically, for the AGATA and GALILEO array detectors. In Fig. 1 a stack is shown of three digitizer cards. The modules can be interconnected using the provided backplane connectors, which distribute the power supplies, the clock signal, and other signals needed for programming and synchronizing the card.



Fig.1. A stack is shown of three digitizer cards, able to serve 36 preamplifier channels, i.e. a full set of segment electrodes of an AGATA germanium crystal. Looking at the stack from the front side (a) the six MDR connectors used for the analog input signals can be seen. Looking from the rear side (b) the six installed backplane connectors can be seen. Three of these (on the left) are for the signals (clock, test pattern, I2C, SPI, reset). The remaining ones (on the right) are for power supplies.

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Fig. 2. Simplified schematic diagram of a channel of the analog conditioning circuit. It comprises differential impedance termination, amplification, commonmode and differential DC voltage setting, range selection, external or test-pattern input selection, anti-aliasing filtering. The ADC, model ADC1413D105 (not shown), is connected to the output of the analog chain.

II. ARCHITECTURE OF THE CARD

The card comprises an original analog conditioning chain, high-speed high-resolution differential flash ADC's with integrated JESD204A encoder [8], and an optical transmitter with 12 laser channels. The analog chain features low noise, low power consumption, and wide bandwidth. Moreover it has many useful features, including:

- differential or single-ended analog input,
- end termination for both the differential- and commonmode components of the input signals,
- AC or DC coupling to the ADC,
- introduction of a preset common-mode voltage for differential ADC matching,
- introduction and remotely-controlled adjustment of the differential DC offset, useful for dynamic range maximization,
- remotely controlled dynamic-range selection,
- anti-aliasing filter,
- test-pattern waveform multiplexed at each analog input for precise inter-channel time synchronization,
- optional interleaved mode for equivalent samplingfrequency multiplication.

In Fig. 2 a simplified schematic diagram of the signal path used in the analog conditioning chain is shown. The circuit uses a low-power rail-to-rail dual operational amplifier AD8030 as signal receiver, configured as a low-noise differential buffer amplifier. A preset positive DC commonmode voltage is enforced for ADC matching, as given by the mean value of regulated DC voltages "1.25V_a" and "1.75V_a". Two low-capacitance Single-Pole Double-Throw (SPDT) switches ADG772 are used for range selection and for time calibration. Note that in the proposed solution the parasitic resistance of the SPDT's is not in series to the end termination resistors R1a and R2a, which would severely spoil the gain linearity along the signal path. It is instead in the antialiasing filter path, in such a way to see a high-impedance load at low frequency. This makes its impact on the gain linearity negligible.

Range selection is realized through resistor dividers "R3a-R4a" and "R7a-R8a", as connected between the differentialsignal pairs to the regulated DC voltages "1.25V a" and "1.75V a". Transmission of the split or full signal is selected by properly setting the control inputs of SPDT's "U2a" and "U3a", which work here as analog multiplexers. "U2a" and "U3a" control inputs can be also set in such a way to transmit a test-pattern waveform (Testp a, Testn a) to the ADC input. Such input is intended to measuring the overall time skews and differential latencies among the electronic chains, brought about by the ADC's as well as the optional optical transmitter/receiver pairs. The measurement of the differential delay/latency may be used for time alignment in multi-channel applications, and is essential to attain high resolution in timing and coincidence measurements. The programmable DC voltages "1.25V a" and "1.75V a" provide a differential DC offset to the ADC input signal. Such an offset permits optimal use the ADC input range in all cases when the signals are unipolar, like in nuclear spectroscopy. In such cases in fact as much as half of the range would be unused if no DC offset were introduced in the ADC signal. Note that using such analog conditioning circuit not only is an adjustable DC offset introduced, but it keeps unchanged when the range is changed, i.e. it is not affected by resistor dividers "R3a-R4a" and "R7a-R8a". The DC offset is remotely adjusted through digital potentiometers, easily programmed via an I2C bus interface.

Each DC-offset circuit section (not shown) serves four preamplifier channels. It is based on quad digital potentiometer AD5224 configured in voltage-divider mode, which yields an excellent temperature coefficient of 25 ppm/°C. The circuit provides four pairs (1.25V_a, 1.75V_a), (1.25V_b, 1.75V_b),



Fig.3. Digitized preamplifier signals from detector "MARS"

(1.25V_c, 1.75V_c), (1.25V_d, 1.75V_d), each of which has mean value of 1.5V. Adjustment of the DC offset modifies differentially the voltages of each pair, while leaving unchanged their mean value at 1.5V. The circuit yields individually adjustable DC offsets superposed to the ADC signals. The optimal values for the DC offsets can be saved in dedicated non-volatile memory cells embedded in AD5224 chip.

The circuit permits optionally to distribute the same analog signal to two ADC's by means of balanced splitters. Clocking the ADC's in phase opposition and combining the recorded waveforms yields interleaved operation. Using such interleaved mode the effective sampling frequency gets doubled. The analog circuitry works on a single 3.3V power supply with a static power consumption of only 20mW/channel.

Six dual flash ADCs are used, each with two integrated serialized outputs. Each lane is differential and complies with the JESD204A standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADCs. The ADC's use 3V and 1.8V power supplies. Pin-to-pin compatible ADC's are available with resolutions of up to 16 bit and clock frequencies of up to 125 MS/s.

The serialized ADC outputs are sent to a SNAP12 optical transmitter for final transmission of the full data stream to the



Fig.4. Statistical properties of the digitized preamplifier signals as analyzed on the baseline.

remote user.

Overall a digitizer card needs a 3.3V and a 2.0V power supplies, sinking about 2.5 and 0.6 A, for an overall power consumption of only \sim 10W, i.e. \sim 0.8W/channel including the laser.

III. EXPERIMENTAL RESULTS

In Figs. 3, 4, 5, and 6 the first native and filtered digitized waveforms collected from real detector signals are shown. We used the segmented germanium detector "MARS" [9]-[11] for data generation with an advanced charge preamplifier [12]-[22] and the AGATA local processing digital electronics for filtering and analyzing the signals [7]. All shown data have been collected by the local-processing modules through the same optical-fiber link used in AGATA. Figs. 3 and 4 show the native digitized signals as seen at the detector/preamplifier output. The shape of the signals is a clean exponential decay as expected and no artifacts are observed. The noise as measured on the baseline of the preamplifier signals is 230 µV r.m.s., i.e. 1.89 LSB r.m.s. After the trapezoidal digital filter [23], however, most of the noise is filtered out. In fact as can be seen in Figs. 5 and 6 the baseline of the trapezoidal signal as represented in a 16-bit numerical format shows a noise of 0.5



Fig.5. An event as seen after the trapezoidal digital filter.



Fig. 6. Statistic properties of the filtered signal as analyzed on the baseline.



Fig.7. Eye diagram of the encoded and serialized 2Gb/s digital signal.

LSB r.m.s., even smaller than the 2-bit tighter quantization step. Note that the quantization noise is as well filtered obtaining a bit gain of >2, as is typical in these systems, when properly optimized [24]-[33]

In Fig. 7 the eye diagram is shown of the 2 Gb/s encoded and serialized signal provided by one ADC channel as measured using a 7GHz high-impedance differential probe and a 12GHz oscilloscope. As can be seen the eye diagram is well open, which reveals the correct operation at high frequencies of the electrical system. All 12 such eye diagrams have been checked as probed on the corresponding input pin pairs of the optical transmitter module, and look pretty similar to each other.

In Fig. 8 the first ⁶⁰Co spectrum collected with the full chain is shown. In the inset pictures of the detector and the digitizer are shown. The line width is 2.6 keV fwhm, as expected considering that the input FET (Field Effect Transistor) was operated at room temperature and moreover we could not deplete fully the detector because of a vacuum leak in the cryostat. Other measurements will be performed with an AGATA capsule as soon as it will be available for these tests.

IV. REFERENCES

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Fig.8. Spectrum of ⁶⁰Co from the front electrode of germanium detector "MARS" as obtained using the described digitizer.

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