A Digital Signal Processing Module for Time-Division Multiplexed Microcalorimeter Arrays

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***Abstract*—We have developed a digital signal processing module for real time processing of time-division multiplexed data from SQUID-coupled transition-edge sensor microcalorimeter arrays. It is a 3U PXI card consisting of a standardized core processor board and a daughter board. Through fiber-optic links on its front panel, the daughter board receives time-division multiplexed data (comprising error and feedback signals) and clocks from the digital-feedback cards developed at the National Institute of Standards and Technology. After mixing the error signal with the feedback signal in a field-programmable gate array, the daughter board transmits demultiplexed data to the core processor. Real-time processing in the field-programmable gate array of the core processor board includes pulse detection, pileup inspection, pulse height computation, and histogramming into on-board spectrum memory. Data from up to 128 microcalorimeter pixels can be processed by a single module in real time. Energy spectra, waveform, and run statistics data can be read out in real time through the PCI bus by a host computer at a maximum rate of ∼100 MB/s. The module's hardware architecture, mechanism for synchronizing with NIST's digital-feedback, and count rate capability are presented.**

***Index Terms*—Data acquisition, digital signal processing, time-division multiplexing, transition edge sensor.**

I. Introduction

MULTIPLEXED READOUT of large arrays of transition edge sensor (TES) x-ray or gamma-ray microcalorimeters coupled to superconducting quantum interference devices (SQUIDs) have been demonstrated in recent years [1]–[3]. These TES x-ray or gamma-ray microcalorimeters have the potential to be used as high-energy-resolution, high-count-rate x-ray or gamma-ray spectrometers for applications in astrophysics, materials analysis, nuclear forensics and international nuclear safeguards [4].

The National Institute of Standards and Technology (NIST) in Boulder, CO has developed a time-division multiplexed (TDM) SQUID readout system for large-format TES arrays [5], [6]. A key component of this TDM readout system is a digital-feedback (DFB) card developed at NIST. The DFB card digitizes a multiplexed signal from a column of the array and maintains a flux-locked loop for each column. The feedback and error signals computed by the DFB are serially streamed to the host computer through a fiber-optic link between the DFB and a NIST-developed PCI card installed in the computer. The captured feedback and error data can then be analyzed offline via optimal filtering to compute pulse energies.

For large microcalorimeter arrays, the amount of data that needs to be streamed and stored becomes prohibitively limited by the available data bandwidth. Therefore, real time processing of microcalorimeter pulses in the readout electronics and only transmitting and storing a limited data record for each event in the computer should help greatly, particularly in high-count-rate applications. While hardware based real time processing of microcalorimeter pulses using optimal filtering has been reported [7], count rate capability in such applications is limited.

XIA has developed digital pulse algorithms that can not only be implemented in a digital signal processing module but also achieve comparable energy resolution to optimal filtering with TES detectors [8], [9]. In addition, we have reported a versatile digital signal processing (DSP) module that consists of a standard main processing board and a variety of readout-specific daughter boards [10]. In this paper, we report a new DSP module, the MicroCAL-T128, whose daughter board was specifically designed for interfacing to the NIST DFB cards for real time processing of TDM data. We first describe its hardware architecture, then discuss the mechanism that we use to synchronize the DFB with the MicroCAL-T128, and finally report its count rate capability.

II. Hardware Architecture of the MicroCAL-T128

As shown in Fig. 1, a MicroCAL-T128 pulse processing board consists of a TDM daughter board (top) and a standard main board (bottom), forming a single-slot width 3U PXI module that can be operated from a PXI chassis. Power is supplied from the main board to the daughter board through an inter-board power connector, and data communication between them is done via high-density board-to-board connectors.

Fig. 2 shows the block diagram of the MicroCAL-T128 TDM daughter board. Its front end features six fiber-optic receivers (HFBR-2526Z), which accept up to six fiber-optic connections from the NIST DFB system. The six HFBR receiver outputs are then sent to six limiting amplifiers (MAX3645) that function as data quantizers with loss-of-signal (LOS) detectors and output differential positive emitter coupled logic (PECL) signals to

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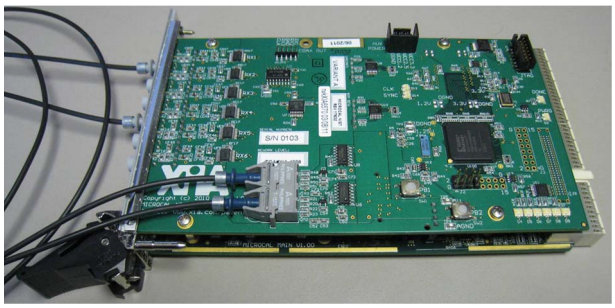

Fig. 1. Picture showing a MicroCAL-T128 board consisting of a TDM daughter board and a main board.

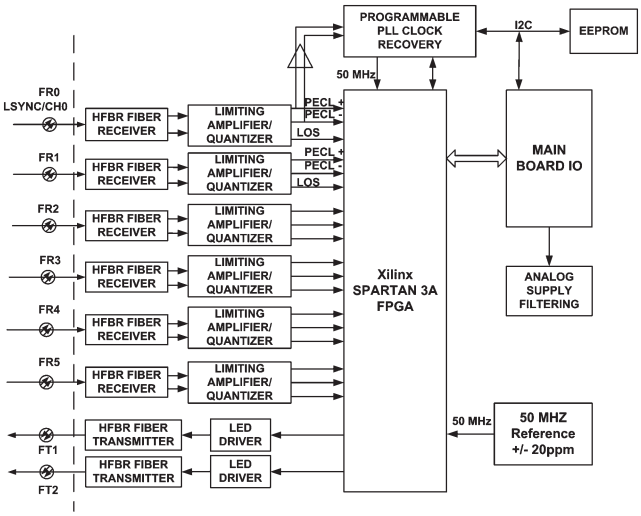

Fig. 2. Block diagram of the MicroCAL-T128 TDM daughter board.

the Xilinx Spartan 3 A FPGA (XC3S400A-4_C_BGA320). Additionally, the output from one limiting amplifier (typically the first one) that is associated with the LSYNC signal, a periodic pulse sent by the NIST's clock card [5], is also sent to a programmable Phase Locked Loop (PLL) (FS1745) for clock recovery. The recovered 50 MHz clock is then sent to the FPGA allowing it to capture data synchronously from other fiber-optic receivers.

III. MicroCAL-T128 Interface and Hardware Functions

A. Interface Overview

The MicroCAL-T128 board accepts two types of signals from NIST's DFB system through fiber-optic cables: one is the LSYNC, whose period is the master clock period divided by N_{CLK} ($N_{\mathrm{CLK}} \geq 32$), and the other is 32-bit data packets, which consist of 14-bit feedback and 16-bit error signals, an overflow bit and a data-framing bit.

The synchronization between NIST's DFB system and the MicroCAL-T128 consists of three steps: 1) recover the 50 MHz master clock in the MicroCAL-T128 using the LSYNC; 2) synchronize data packets relative to LSYNC edges using reference pattern matching (bit sync); and 3) determine the starting frame by searching for the frame bit "1".

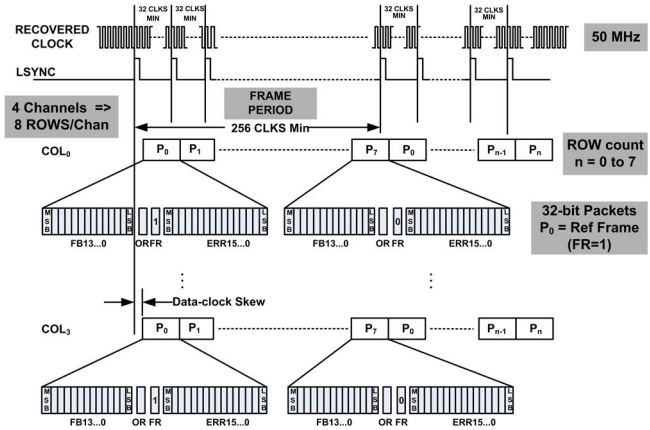

Fig. 3. Timing diagram for the MicroCAL-T128 daughter board.

B. Clock Recovery

In order to synchronously capture data from the DFB cards, it is necessary to recover a 50 MHz clock from the LSYNC since the LSYNC is synchronous with the data from the DFB cards and the local 50 MHz clock on the MicroCAL-T128 board can not be used as it does not necessarily have the exactly same frequency as the clock on the NIST clock card. The 50 MHz clock is recovered in two steps. The PLL first locks onto the LSYNC, and then the 50 MHz is generated from this locked signal by multiplying its frequency by N_{CLK}. Several registers written by the user control software are required to properly configure the PLL, and simple Excel spreadsheet is used to generate the appropriate PLL settings, which are then passed to the PLL via the I2C interface. Performance of the phase shifter depends on the PLL reference clock being low jitter so the Xilinx digital clock manager (DCM) can maintain its lock.

C. Data Recovery (Bit Sync)

Each of the six fiber-optic receiver channels has a standalone deserializer based on FPGA dual port RAM which also acts as a 512 deep $\times$ 32-bit FIFO. Any channel's FIFO can be halted and data in the FIFO can be read to the host computer over the SPI interface.

Fig. 3 shows the timing diagram of the MicroCAL-T128 board. For the discussions below, it is assumed that N_{CLK} equals to 32 and the number of multiplexed rows per fiber-optic receiver is 8.

Once a stable 50 MHz clock is recovered from the LSYNC, the MicroCAL-T128 enters into a data recovery or bit sync phase. It starts by identifying a known data word that is a reference pattern set by the NIST DFB and which is also known to the software at setup. The FPGA detects this pattern to establish a phase relative to the LSYNC. Therefore, the data versus clock skew, whose value is determined by the DFB firmware, can be automatically taken care of by the process of reference pattern matching. Once the reference pattern is identified, the search mode exits to enter a match mode.

D. Frame SYNC Algorithm

The major goal of the match mode is to determine the frame bit "1" in the serial data stream from the DFB. A frame bit

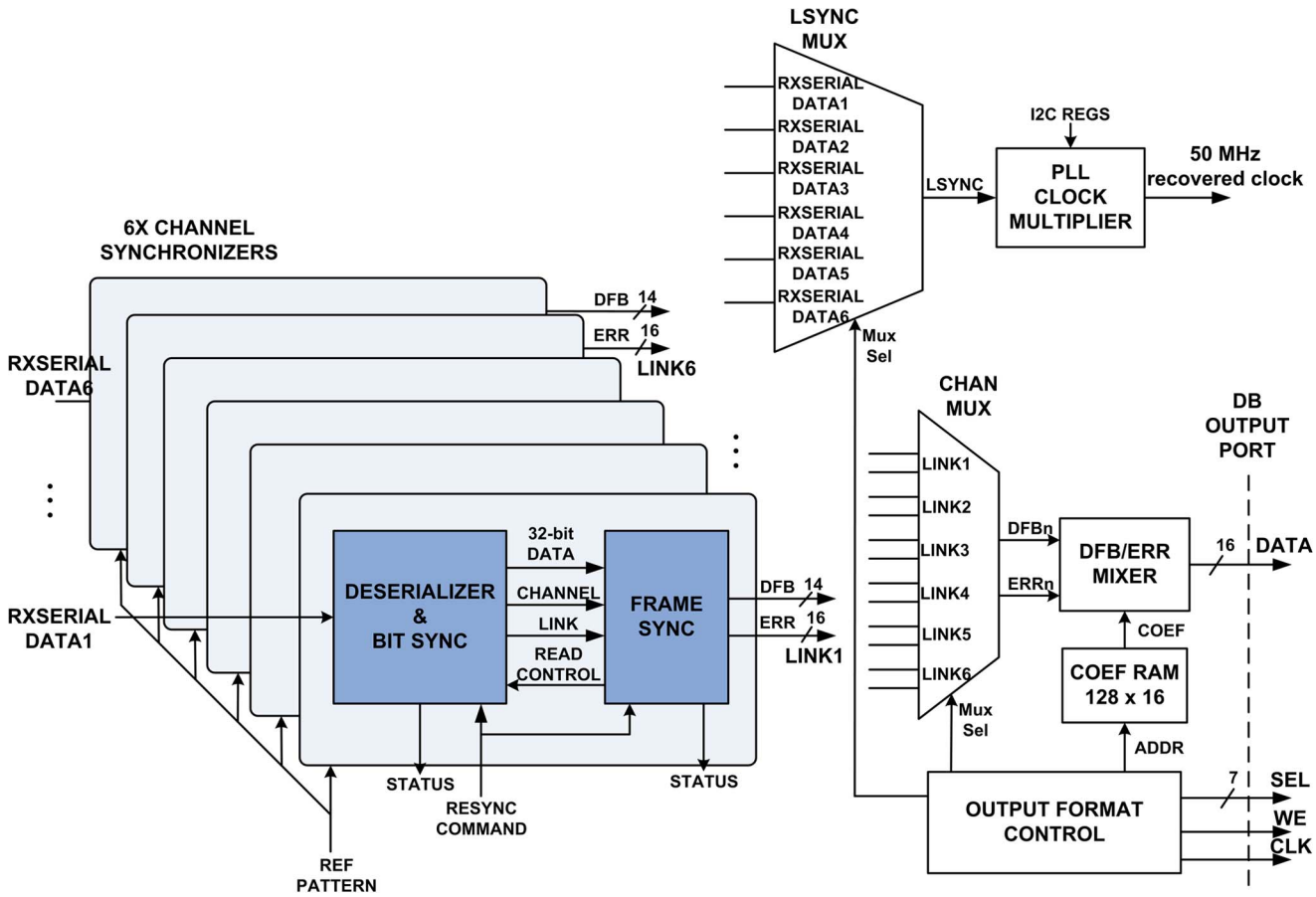

Fig. 4. Functional diagram for the MicroCAL-T128 daughter board.

"1" indicates the starting row of a multiplexed column. One method for finding the frame bit "1" is to observe the successive reference pattern match with the correct period to declare the in-frame condition. Once in frame, the correlator is disabled and the correlator delays are frozen. However, this frame bit "1" is not necessarily present in the reference pattern. Due to this uncertainty a hardware-controlled option is provided so software can disable the test pattern and real data can be provided by the DFB. Alternatively, a backup force mode is provided that simply captures the data pattern and writes it to a register. The correlator delays can then be set manually by software. By repeated monitoring of the received data register, the phase setting can be determined and locked in place for each channel individually.

E. MicroCAL-T128 Functional Diagram

Fig. 4 shows the functional diagram of the MicroCAL-T128. It essentially summarizes the aforementioned hardware architecture and interface functions. For clock recovery, the clock source for the PLL can be any of the six serial data inputs through software selection; but in practice, channel 0, or RXSERIAL DATA1, is typically used.

Signals recovered from the optical to electrical conversion are extracted from the channel of interest as 14-bit feedback and 16-bit error values. The error values are multiplied with an 18-bit coefficient and scaled to 14-bits before addition with the 14-bit feedback value resulting in 15-bit unsigned results. The software writes an 18-bit mix coefficient value to a register in the daughter board FPGA for each channel. The 18-bit coefficient is signed and the error offsets are assumed as well so the correction may be positive or negative although the result is unsigned. A 23-bit data and control bus sends the final 16-bit sample data and a 7-bit index from the TDM daughter board to the main board. A valid strobe is included to indicate valid data synchronously with the 50 MHz system clock.

F. Number of Pixels Supported by Each MicroCAL-T128

The main board FPGA of a MicroCAL-T128 uses an interleaved mechanism to process interleaved data samples from up to 128 microcalorimeter pixels sent by the TDM daughter board. The limit of 128 channels is set by the available FPGA memory resources for that many channels. It takes 8 clock cycles of the FPGA, which runs at 100 MHz, to process each multiplexed sample. This time is needed to retrieve previously stored real-time filtering values for each pixel and then save the updated ones to storage. Therefore, the maximum data rate allowed for the TDM daughter board is 12.5 MHz. If five of TDM daughter board's six fiber-optic receivers are used to accept data from the DFB cards, the maximum packet rate for each fiber is 2.5 MHz, i.e., inter-packet interval should be at least 400 ns.

When 50 MHz master clock is used in the DFB and $N_{\mathrm{CLK}} = 32$, the minimum sampling interval allowed by the DFB is 5.12, 10.24 or 20.48 μs for 8, 16, or 32 multiplexed rows per column,

TABLE I
TOTAL NUMBER OF MULTIPLEXED MICROCALORIMETER PIXELS SUPPORTED BY THE MICROCAL-T128

Number of multiplexed rows for each fiber optic receiver	Number of fiber optic receivers to use		Minimal sample interval limited by MicroCAL-T128 (μs)		Minimal sample interval provided by DFB (μs)		Total number of pixels supported	
	50 MHz master clock	100 MHz master clock	50 MHz master clock	100 MHz master clock	50 MHz master clock	100 MHz master clock	50 MHz master clock	100 MHz master clock
8	5	4	3.2	2.56	5.12	2.56	40	32
16	5	4	6.4	5.12	10.24	5.12	80	64
32	4	4	10.24	10.24	20.48	10.24	128	128

respectively. For 32 multiplexed rows per column, only up to 4 fiber receivers can be used due to the limit of 128 channels. Correspondingly, the minimum sampling interval imposed by the MicroCAL-T128 board is 3.2, 6.4, or 10.24 μs, respectively. Since the minimum sampling interval allowed by the DFB is higher than that imposed by the MicroCAL-T128, it is clear that the MicroCAL-T128 can support up to 128 channels with 50 MHz master clock. In the case of 100 MHz master clock that is used in the new-generation DFB, the same is true as shown in Table I.

G. Theoretical Count Rate Capability

The MicroCAL-T128 board can be operated in two data acquisition modes: multichannel analyzer (MCA) histogramming mode, in which only MCA histograms (64 K bins of MCA histogram storage space for each channel) and counting statistics are accumulated for each channel in real time, and list mode, in which in addition to the histogram and counting statistics data, triggered waveforms can also be recorded. When running in MCA histogramming mode, the output count rate capability will only be limited by the energy filter time, which is settable by a user. For instance, if the energy filter time is set to 100 μs, the output count rate can potentially reach 3,678 cps per pixel or ~470 Kcps for 128 pixels combined.

The list mode data storage space for each of the 128 channels is 131 072 words (16-bit wide). If each triggered record consists of 8192 samples in the form of 32-bit data (both feedback and error data included), each channel can store up to 8 events in its on-board memory. Considering the PCI readout speed of ~100 MB/s, each triggered record has about 32 K bytes of data, and for 128 channels, the total data amount is about 4 MB. So it is possible to capture about 25 counts per second for each of the 128 channels, and that amounts to about 3,200 cps for the whole 128 pixels. If only recording timestamp and energy for each trigger, then the capable output count rate capability can be higher and only subject to the constraint of energy filter time.

IV. HARDWARE TEST

The MicroCAL-T128 board has been tested using its built-in optical transmitters. LSYNC and data signals were first generated in the daughter board FPGA, and then sent to the front panel optical receivers through two on-board optical transmitters, forming a loop-back test. Additionally, in order to test the effect of clock jitter from the PXI crate clock, one MicroCAL-T128 board was installed in one crate and its LSYNC and data signals were then sent to a MicroCAL-T128 board in another PXI crate.

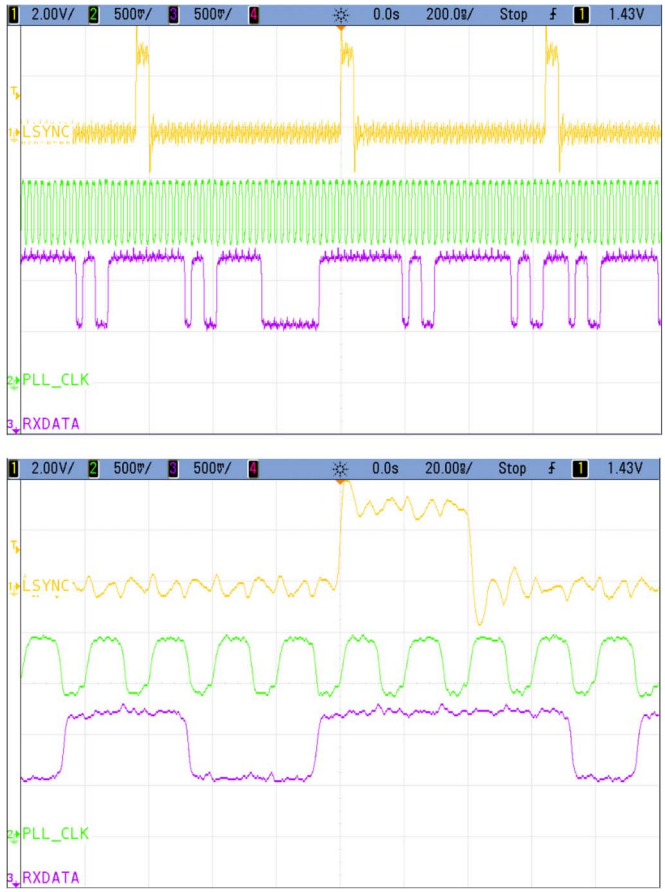

Fig. 5. Timing diagram for the MicroCAL-T128 daughter board.

Fig. 5 shows both the PLL recovered 50 MHz from the input LSYNC signal and the proper alignment of the data with the recovered clock. The recovered clock locks to the LSYNC signal, illustrating the reliability of the clock recovery. The bottom half of the Fig. 5 shows the alignment of the recovered clock rising edge with the center of the data bits. Therefore, it provides sufficient timing margin for proper data sampling.

V. CONCLUSION

A digital signal processing module has been developed for interfacing to the NIST DFB boards for real-time processing of time-division multiplexed microcalorimeter pulses. Each module supports up to 128 microcalorimeter pixels. Thus several modules installed in a 3U PXI crate can process signals from large TES arrays and provide a cost effective solution for reading out such large arrays without the need to store large amount of raw pulse data.

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