AGET, the GET Front-End ASIC, for the readout of the Time Projection Chambers used in Nuclear Physic Experiments

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***Abstract*– Today with the advent of intense radioactive beams, we have access to nuclear spectroscopy and reaction studies of nuclei far from stability. It has been demonstrated that Time Projection Chambers (TPC) method can be very effective as an active target for such studies yielding low thresholds, efficiency and luminosity [1]. To this end a Generic Electronic system for TPCs (GET) is in development and will cover small to medium sized instrumentation (64 to 32 k channels) with a relatively wide charge dynamic ranges for event rates of up to 1 kHz. The 64-channel AGET (ASIC for GET) front-end circuit has been developed to perform the amplification, detection and analog storage of the shaped detector signal before its digitization by an external 12-bit ADC. This design offers a large flexibility in sampling frequency (100 MHz max.), peaking time (16 values from 50 ns to 1 µs), gain (4 ranges from 120 fC to 10 pC per channel) and signal polarity (negative or positive). Fabricated using 0.35 µm CMOS technology, the AGET prototype is under test and the first results are presented.**

I. INTRODUCTION

THe research on exotic nuclei will use the new generation of radioactive ion beams, such as SPIRAL2 at GANIL in France, RIKEN at Wako in Japan or FAIR at Darmstadt in Germany, or rare isotope beam facilities such as NSCL at Lansing in the United States for nuclear spectroscopy. These nuclear experiments require highly efficient detection. TPCs are very attractive for the measurement of nuclear reaction processes occurring between beam particles and the nuclei of the gas in detector chambers. The main characteristics being sought is to reduced energy threshold yet retaining a high luminosity and a large solid angle without compromising the energy and angular resolution.

To read these TPCs, the nuclear physics community (ACTAR (GANIL), TPC2-BX (CENBG), AT-TPC (NSCL) [2] (Fig. 1), SAMURAÏ-TPC (RIKEN)) has decided to develop a complete electronic system called GET [3], financed by French and American agencies (ANR and NSF) with the ambition to be a versatile tool for medium sized instrumentation (32 k channels maximum).

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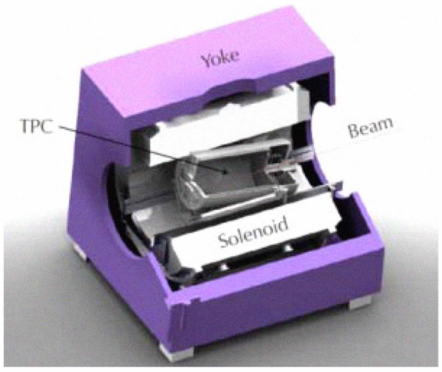

Fig. 1. Conceptual design of the AT-TPC.

II. OUTLINE OF THE GET ELECTRONIC

The aim of GET is to design a generic electronic system from the front end to data storage, focusing on TPCs. Fundamentally, a TPC consists of a drift chamber with an electric field oriented parallel to an external magnetic field. Charged particles from a nuclear reaction produce an ionizing track as they cross the volume of the detector. Under the influence of the electric field the secondary electrons drift towards the anode wires where they are amplified and recorded by readout pads. The amount of charge and the time of arrival of the signal are recorded allowing a 3-dimensional reconstruction of the path of the ionizing particle. The radius of curvature of the track is used in conjunction with the energy deposit to identify particle species. To measure these parameters, each pad signal will be recorded over a duration slightly larger than the maximum TPC drift time or compatible with multi-events detection. This task is achieved by the AGET ASIC based on the previously developed AFTER ASIC [4] enhanced with significant new features and modifications to match different detectors (gain and drift time), to discriminate the detector signal (multiplicity signal for building trigger, hit channel address for selective readout), to decrease the dead time (selective readout, 1 to 512 SCA cells) and to cope with specific nuclear decay mode, e.g. 2-proton radioactivity in TPC2-BX project (SCA split in two to allow consecutive pulse recording of a nuclear decay).

Four of these circuits (Fig. 2) are soldered on the AsAd (ASIC Support & Analog-Digital conversion) card with a 4-channel 12-bit ADC (one per AGET). The digital outputs of the 4-ADC are transmitted via 8 differential lines with a maximum speed of 1.2 Gbit/s to the CoBo board. The CoBo

(Concentration Board) board is responsible for applying time stamp, zero suppression and compression algorithms to the data. In addition it serves as a communication intermediary between the AsAd boards and the outside world. The slow control signals and commands to the AsAds are transmitted via the CoBo (four AsAD per CoBo).

MuTanT (Multiplicity Trigger And Time) card issues a three level trigger via the external trigger, multiplicity and the event pattern. It manages also the clock distribution over the whole system. CoBo and MuTanT are set in microTCA crate [5]. Data are transmitted through a 10 Gb-Ethernet network to the computer farm.

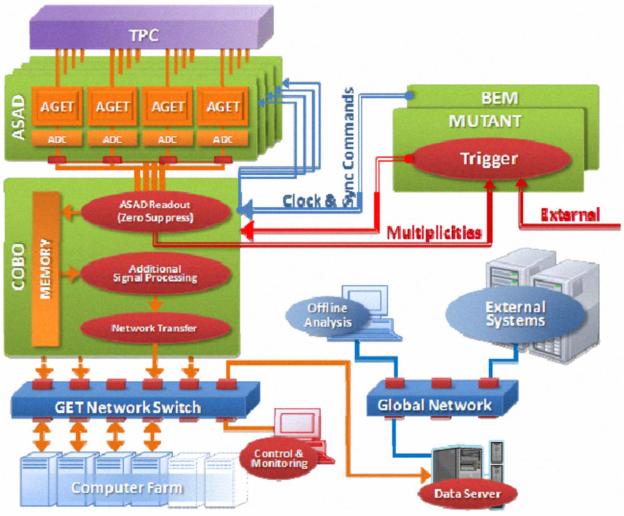

Fig. 2. TPC module readout architecture.

The BEM (**B**ack-**E**nd **M**odule) card must ensure the interface between the GET electronics and other ancillary equipment used in nuclear physics experiments (charged-particle and gamma-detector arrays, spectrometers).

The data acquisition system is based on NARVAL [6] and slow control firmware is resident in each CoBo.

III. THE AGET ASIC

The AGET chip includes 64 channels (Fig. 3) each handling one detector pad. A channel integrates mainly: a charge sensitive preamplifier, an analog filter (shaper), a discriminator for multiplicity building and a 512-sample analog memory.

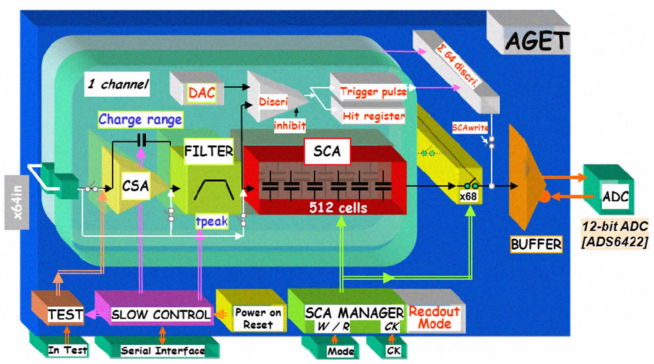

Fig. 3. Architecture of the AGET chip.

The charge sensitive preamplifier (CSA) has a variable gain to support the dynamic range of 120 fC to 10 pC. This gain is adjustable for each channel, by selecting one of the four CSA feedback capacitors. The analog filter is formed by a Pole Zero Cancellation stage followed by a 2-complex pole Sallen-Key low pass filter. The peaking time of the global filter is selectable among several values (16 values) in the range of 50 ns to 1 µs. The filtered signal is sent to the analog memory and discriminator inputs.

The analogue memory is based on a Switched Capacitor Array structure (SCA), used as a 512-cell deep circular buffer in which the analog signal coming out from the shaper is continuously sampled and stored. The sampling frequency can be set from 1 MHz to 100 MHz to match the various drift velocities in chambers. The sampler is stopped on an external trigger decision. In the readout phase, the analog data from the different channels is multiplexed toward a single output and sent to the external 12-bit ADC at the readout frequency of 25 MHz. Three different readout modes are available: all channels, or only hit or specific channels. In conjunction with this channel readout mode, it is possible to read only a predefined number of analog cells (1 to 512) starting from an index defined with a constant offset from the cell corresponding to the trigger arrival.

The filtered signal, after being amplified by a differential gain stage, is compared by the discriminator to a programmable threshold value. This voltage is set by programmable 8-bit DACs. The first four bits (polarity and 3 MSBs) are common to the 64 channels whereas the 4 LSBs can be tuned for each individual channels. When the signal crosses the threshold, the discriminator output signal sets the hit channel register to an active level and forms with the 63 others discriminator signals a multiplicity signal (analog sum) which duration can be either the time over threshold or fixed to a predefined value depending on the AGET configuration. During the SCA writing phase, this signal is continuously digitized by the external 12-bit ADC used for the analog output and analyzed in real time to build a trigger signal.

The hit-channel register is set by the output signal of the discriminator and reset after a programmable time (4 values) which is comprised between a quarter and two SCA complete depths. If a second event comes, the memory time is increased again by the same previous value. This hit-channel register can be readout or modified after the SCA write phase by using AGET slow control lines with a specific high speed protocol.

To process two consecutive events (implantation & decay event) in a time window less than 1 or 2 ms, it is possible, by slow control configuration, to split the SCA memory (Fig. 4) in two separate blocks.

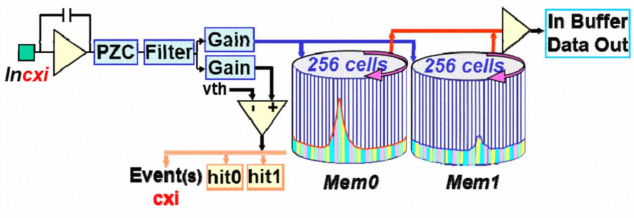

Fig. 4. The SCA can be split in two separate memories of 256 cells.

Each block is dedicated to sample and store its own event until the readout phase in which both memory blocks will be read out consecutively.

An SPI compatible serial link allows the configuration of the chip parameters (e.g. gain, peaking time, test, readout mode). Two chip inputs allow users to calibrate or test the channels. To cope with the various detector configurations, the ASIC can operate with both signal polarities depending on which DC voltages inside the ASIC are adjusted.

It is also possible to bypass the internal CSA of the channel and to enter directly into the filter or SCA inputs through an external CSA.

The AGET requirements are reported on Table 1.

TABLE I. SYNTHESIS OF AGET REQUIREMENTS

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC Adjustable per channel
Output dynamic range	2 V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120 fC; Peaking Time: 200 ns; Cdetector < 30 pF)
Peaking Time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2x256 cells
Sampling frequency	1 MHz to 100 MHz
Readout frequency	25 MHz
Multiplicity signal	Analog "OR" of 64 discriminator outputs
Threshold value	4-bit DAC/channel + 4-bit DAC
Channel readout mode	Hit, selected or all
Test	1 among 64 channels or all
Power consumption	< 10 mW / channel @ 3.3 V

IV. TEST OF THE FIRST AGET PROTOTYPE

The AGET circuit has been manufactured in the 0.35µm CMOS AMS process. The chip area (Fig. 5) is 8.5 x 7.6mm^2, including more than 700,000 components. AGET is housed in a LQFP 160-pin package, compatible pin to pin with the AFTER ASIC.

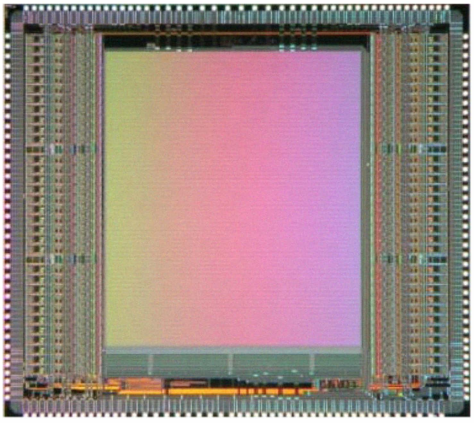

Fig. 5. AGET die photography, size 8.5 x 7.6 mm^2.

The complexity of the chip and its large number of operation modes call for an optimal test acquisition system. We have chosen to use the prototype of the AsAd card as test board (Fig. 6) and the CoBo card as acquisition device in its reduced version (ML507 Evaluation Platform from XILINX). The development and the functionality of this test bench (hardware, firmware, and software) have introduced some delay on the test of the first prototype of the chip.

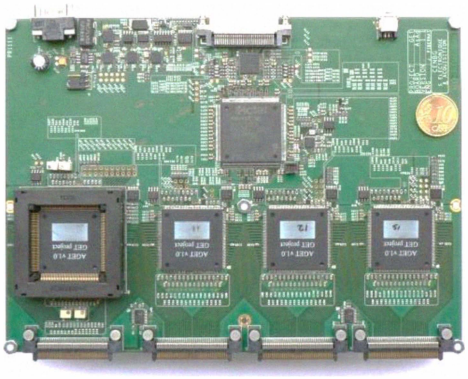

Fig. 6. The AsAd card for the AGET test.

Several tests have been also done on the chip by using the AFTER test bench to control the global functionality of the chip and to perform performances analysis. The measured power consumption of the chip ranges from 9.12 mW to 10.31 mW per channel depending on the bias current of the CSA input transistor (400 µA or 800 µA).

A. Signal Shape

The filter integrated in AGET is a CR-RC^2 with two complex poles providing a quasi-semi Gaussian shape. The Fig. 7 shows the response of the chip to generator pulses injected through the test input for 5 different peaking times (100 ns, 200 ns, 500 ns, 700 ns & 1 µs) and sampled in the SCA at 100 MHz.

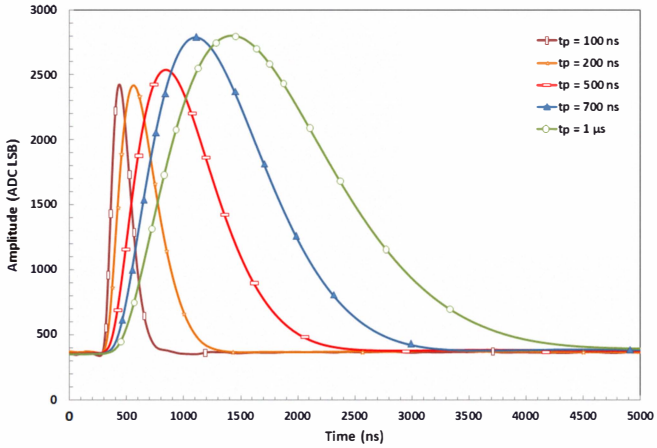

Fig. 7. The test pulses recorded by AGET (120 fC range).

The timing parameters of the pulses measured for the 16 peaking time values, reported in the Table II, are consistent with the simulation results. In this table, T_{peak} is the signal rise time measured from 5% of the full amplitude to the peak, T_{fall} is the signal fall time measured from the peak to 5% and T_{FWHM} is the signal width measured at 50% of the signal amplitude.

TABLE II. MEASURED TIMING PARAMETERS OF THE SHAPED PULSES

Filter peaking Time (ns)	T_{peak} (5%-100%) (ns)	T_{fall} (100%-5%) (ns)	T_{FWHM} (ns)
50	75	130	100
100	110	270	175
200	230	580	390
250	270	710	460
300	330	810	550
350	370	920	620
450	470	1250	820
500	520	1370	890
550	540	1290	920
600	580	1390	980
700	690	1670	1170
750	740	1800	1220
800	790	1960	1340
850	820	2060	1400
950	940	2400	1590
1000	960	2500	1650

B. *Transfer function and Linearity.*

Measurements have been made to extract the different transfer functions (4 gains per channel) by using the pulse generator housed on the test board. An electrical charge is generated by applying a voltage step on an external capacitor (4.8 pF) connected to the input of the selected channel. The maximum amplitude of the signal is recorded versus the input charge as plotted in Fig. 8 (obtained for the 120 fC range).

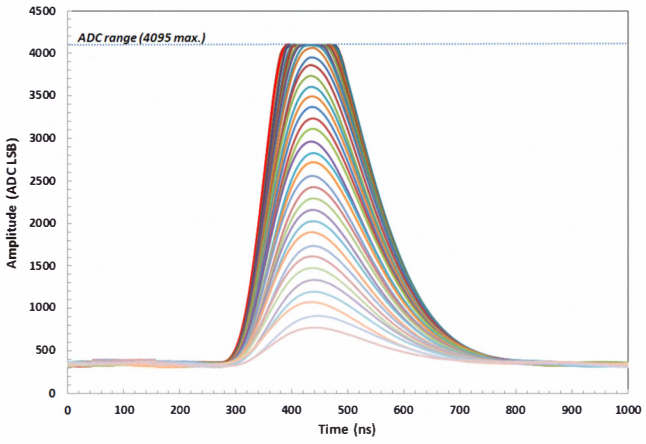

Fig. 8. Output amplitude versus input charge (120 fC range, 110 ns peaking time, 100 MHz SCA write frequency).

The measured values are summarized in Table II and are close to the simulated ones (- 13% to + 1.9%). The highest value of the deviation (- 13%) is obtained for the lowest range which is more sensitive to the effect of parasitic capacitors on the 120 fF of CSA feedback capacitor.

TABLE II. AGET TRANSFER FUNCTION (110 NS PEAKING TIME)

Range (fC)	Simulated (mV / fC)	Measured (mV / fC)
120	17	14.8
240	8.88	8.32
1000	1.864	1.89
10,000	0.1874	0.191

The chip Integral Non Linearity (INL), calculated as the normalized residues to a linear fit of the measured gain, is smaller than 1.2 % over the full chip dynamic range for the 1 pC range or 1.6 % for the 10 pC range (Fig. 9). These results are obtained for 110 ns of peaking time at 100 MHz of SCA write frequency and are better than the 2% specification.

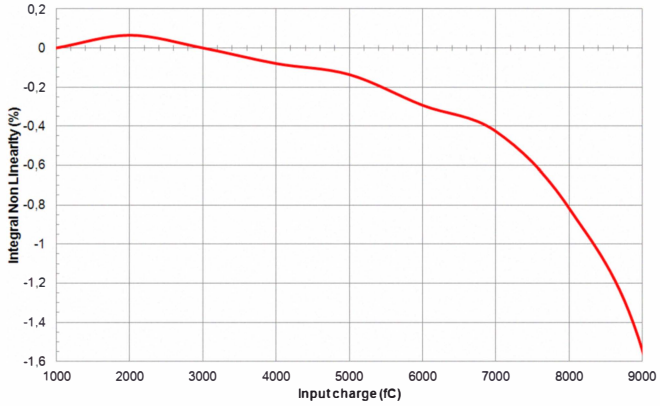

Fig. 9. Integral Non Linearity versus input charge (10 pC range, 110 ns peaking time, 100 MHz SCA write frequency).

C. *Noise measurements.*

The noise of the chip has been measured only for the 120 fC range. Channel 14, located at the center of the left side of the chip has been studied for various peaking times and for different values of the capacitor (simulating the detector) connected at the channel input. The value of Cin = 0 pF is corresponding to the case where the channel input is unsoldered from the test board. The Equivalent Noise Charge (ENC) measured is plotted on the Fig. 9.

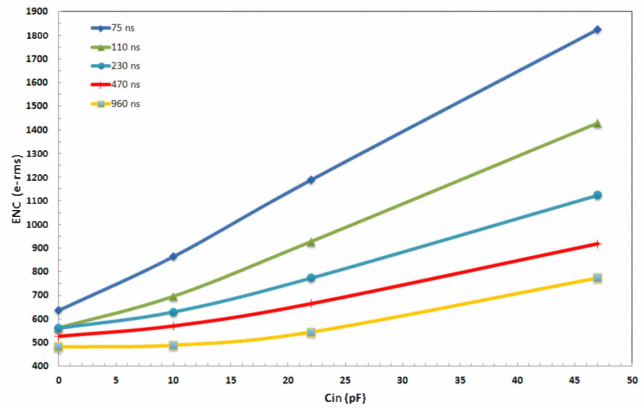

Fig. 9. ENC versus input capacitance for different peaking times (120 fC range, 100 MHz SCA write frequency).

A noise of 900 e- has been measured for Cin = 30 pF and a peaking time of 230 ns. It exceeds by 100 e- the requirements and by 150 e- the value measured on the AFTER ASIC. This extra noise can be explained by 2 factors. The first is the resistor of 10 Ω placed in series at the channel input to protect it against TPC sparks (this resistor doesn't exist in the AFTER chip). The second comes by a possible larger contribution of the chip digital part which is much more complicated and

active in this new ASIC. The noise can be reduced by increasing the current of the CSA input transistor and by minimizing the contribution of the power supplies. This will be done in the next weeks together with the characterization of the chip on the 3 other charge ranges.

D. The SCA 2-memory mode.

Another important functionality of the chip is the possibility to split the SCA memory into two separate blocks of 256 memory cells. This mode has been tested successfully by injecting two charges distant in time by a value greater than the one needed to sample a whole SCA of 512 cells. These 2 sampled signals, shown on Fig.10, are observed using an oscilloscope at the external 12-bit ADC input.

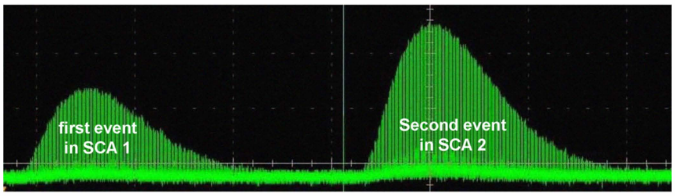

Fig. 10. Readout of the SCA memory configured in 2 x 256 cells. Signal observed using an oscilloscope at the external ADC input. The delay between the two injected charges on the 64 channels (event 1 & event 2) is greater than the sampling time of the total SCA depth (512 cells).

V. CONCLUSION

The AGET circuit is the front end ASIC of the GET electronics project designed to read the endplate detector of TPCs, 3D trackers and active targets in the next generation nuclear physic experiments. The first prototype is under test and results realized so far are very encouraging. The self-triggering functionality was in part tested (hit channel register writing and reading, inhibition, etc.) and the multiplicity signal building remains to be done (minimum threshold value, transfer function, etc.). The end of the full characterization of the AGET chip is expected for early 2012.

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