Digital Readout Electronics for Microcalorimeters

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***Abstract*– Microcalorimeters are cryogenic radiation detectors that measure the energy of incident photons or particles by the increase of temperature in an absorber. They are capable of achieving ultra-high energy resolution, but only with small active volumes and pulse decay times in the order of milliseconds. Consequently, detection efficiency per detector is very low. A practical detector thus requires a large array of microcalorimeters, and either time-domain or frequency domain multiplexing is used to minimize the number of leads exiting the cryostat to room temperature signal processing. Existing readout electronics generally stream the multiplexed data onto a computer hard drive for offline processing. XIA LLC is developing digital microcalorimeter readout electronics that offer real time signal processing. The electronics consist of two major parts: a set of daughter cards and a standardized core processor board. Each daughter card is designed to interface a specific type of microcalorimeter (individual outputs, time multiplexed, frequency multiplexed, etc.) to the core processor. The combination of the standardized core plus a set of easily designed and modified daughter cards allows the design to not only meet present detector signal processing requirements but also ensure future expandability to as yet unspecified detector systems. In this paper, we first present the general architecture of the daughter cards and the core processor board. Then we describe the detailed hardware implementation of the core processor board and of the daughter card with analog inputs.**

I. Introduction

MICROCALORIMETERS are cryogenic radiation detectors that measure the energy of incident photons or particles by the increase in temperature of an absorber. Operating at temperatures of ~0.1 K, the thermal sensor is typically either a thermistor or a superconducting transition edge sensor (TES). Microcalorimeters can be used as very precise detectors for X-ray, gamma-ray, neutron, or alpha particle, since their energy resolution is fundamentally limited only by the ratio of the measured temperature rises to the value of thermodynamic temperature fluctuations. For example, a microcalorimeter for gamma-ray spectroscopy can achieve a resolution of 22 eV (FWHM) in the energy range of 100 keV [1].

The size of cryogenic gamma-ray detectors that can achieve such energy resolutions is limited to ~1 mm^3 per pixel and therefore their detection efficiency is very low. In addition, the maximum count rate is limited by the slow thermal decay time and the currently used "optimum filter" pulse processing algorithms that require isolated pulses to measure pulse heights. These challenges can be partially addressed by fabricating large detector arrays with $10^2 – 10^3$ or more pixels, and either time-domain or frequency domain multiplexing is used to minimize the number of leads exiting the cryostat to room temperature signal processing. However, the increased number of channels in turn requires that the pulse processing be performed as much as possible at the front end of the electronics to avoid transferring large amounts of waveform data to a host computer for offline processing, as is presently the standard practice for small arrays or single detectors.

XIA LLC is developing digital microcalorimeter readout electronics that offer real time signal processing of the multiplexed or non-multiplexed microcalorimeter pulses. The electronics consist of two major parts: a set of daughter cards and a standardized 3U cPCI/PXI core processor board. One daughter card and one core processor board form one complete processing board that occupies a single slot of a standard 3U cPCI/PXI crate. Each daughter card is designed to interface a specific type of microcalorimeter (individual outputs, time multiplexed, frequency multiplexed, etc.) to the core processor. The combination of the standardized core plus a set of easily designed and modified daughter cards allows the design to not only meet present detector signal processing requirements but also ensure future expandability to as yet unspecified detector systems.

We first present the general architecture of the daughter cards and the core processor board, demonstrating the data flow from the daughter cards to the core processor. Then we describe the detailed hardware implementation of the core processor board. We conclude with the description of the daughter card with analog inputs as an example of the three daughter card options.

II. Hardware Architecture

Fig. 1 shows the architecture of the microcalorimeter core processor board and three daughter card options. There are three daughter card variants that are to be built. Option A is for microcalorimeters with individual analog outputs [2]. Option B is for time-domain multiplexed inputs, e.g., NIST's Digital Feedback Board (DFB) [3]. Option C is for connecting directly to digital outputs, e.g., LBL/LLNL frequency-domain de-multiplexed digital outputs [4]. Options A and B include a Format FPGA (optional for option C) which converts the serial data stream into a 16-bit, 8MHz data stream to be sent to the core processor board. Option C uses LVDS receivers to convert the LVDS serial data stream into a 16-bit parallel, 8.4 MHz data stream. At the center of the core processor board is the core processor FPGA that will be capable of processing the multiplexed detector channels in real time.

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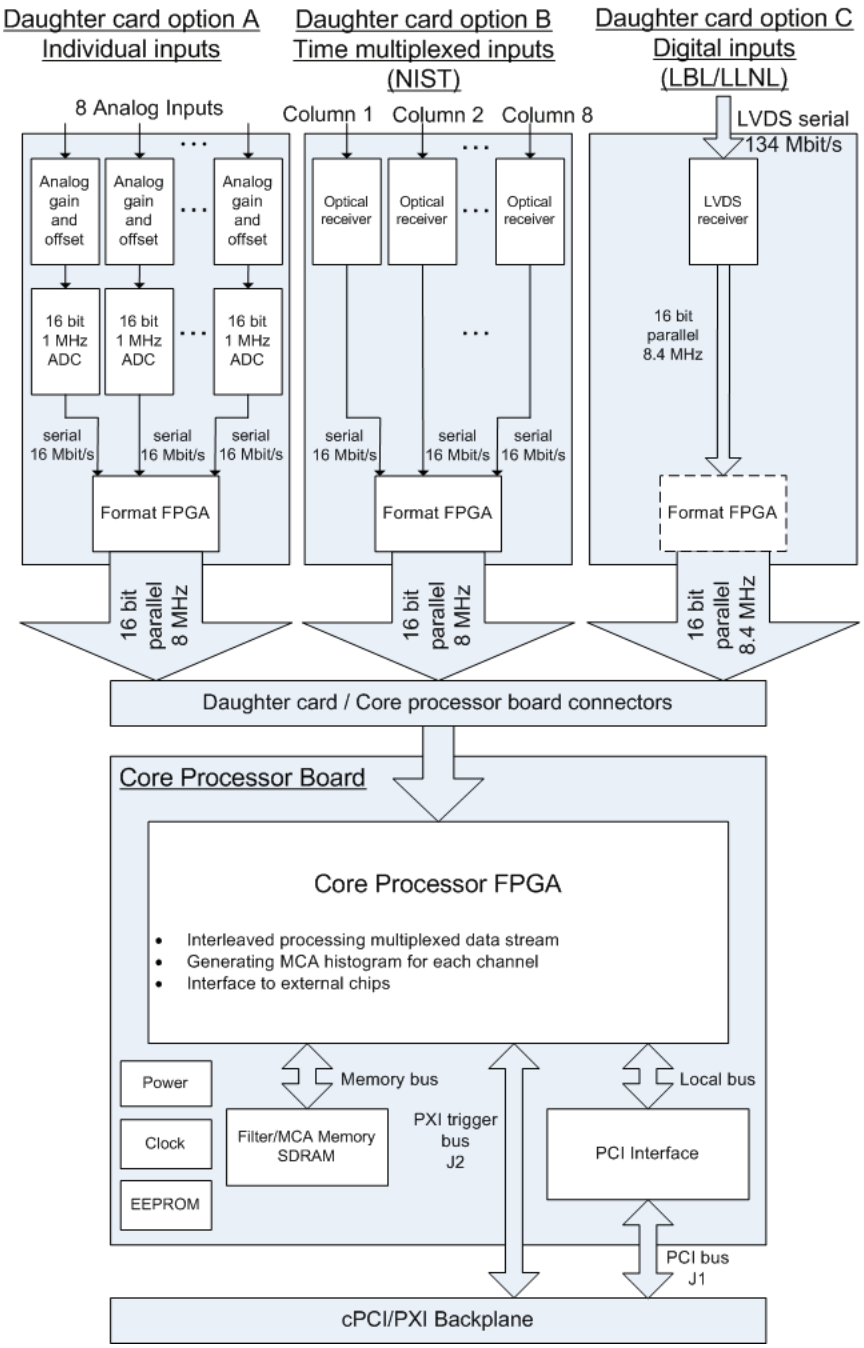

Fig. 1. Diagram of core processor board and three daughter card variants.

TABLE I. TYPICAL DAUGHTER CARD DATA RATES FOR DIFFERENT TYPES OF MICROCALORIMETER DETECTORS

Microcalorimeter Detector Type	Typical Pulse Rise Time	Typical Pulse Decay Time	ADC (16-bit) Sampling Speed	Number of Supported Channels per Daughter Card	Daughter Card to Core Processor Data Transmission Rate
X-ray	10 μs	100 μs	1 MHz	~10	~10 MHz, 16-bit
Gamma-ray	100 μs	1 ms	100 kHz	~100	~10 MHz, 16-bit
Neutron	1 ms	10 ms	10 kHz	~1000	~10 MHz, 16-bit

The data rate transmitted from a daughter card to a core processor board can be determined by each channel's ADC sampling speed and the number of channels that the card will support.

The ADC sampling speed has to be determined based on the specific microcalorimeter detector type. This is because different microcalorimeter detectors have different pulse rise time and decay time. Table I lists typical daughter card

numbers for different types of microcalorimeter detectors. X-ray detectors typically produce pulses with rise time on the order of 10 µs and decay time on the order of 100 µs. To preserve the ultra-high energy resolution of the X-ray detectors, the X-ray pulses have to be digitized at sampling speed of at least 1 MHz. At such sampling speed, 16-bit ADCs are readily available and should be used to achieve the ultra-high energy resolution by reducing the differential non-linearity which is typically associated with ADCs of fewer bits, and by utilizing the high dynamic range of the 16-bit ADCs. Pulses from gamma-ray detectors are approximately a factor of 10 slower than X-ray detector pulses, so 100 kHz 16-bit ADCs can be used for gamma-ray detectors. Similarly, neutron detector pulses are approximately a factor of 10 slower than gamma-ray detector pulses, thus ADCs as slow as 10 kHz can be used there.

The number of channels that a daughter card can support is closely related to the ADC's number of bits and sampling speed. By design, a core processor board can process a continuous 10 MHz 16-bit data stream. Therefore, the maximum number of channels that can be supported by a daughter card is 10, 100 and 1000 for X-ray, gamma-ray and neutron detectors, respectively. The specific types of signal connectors to the daughter card might limit the actual number of channels that can be put on a daughter card.

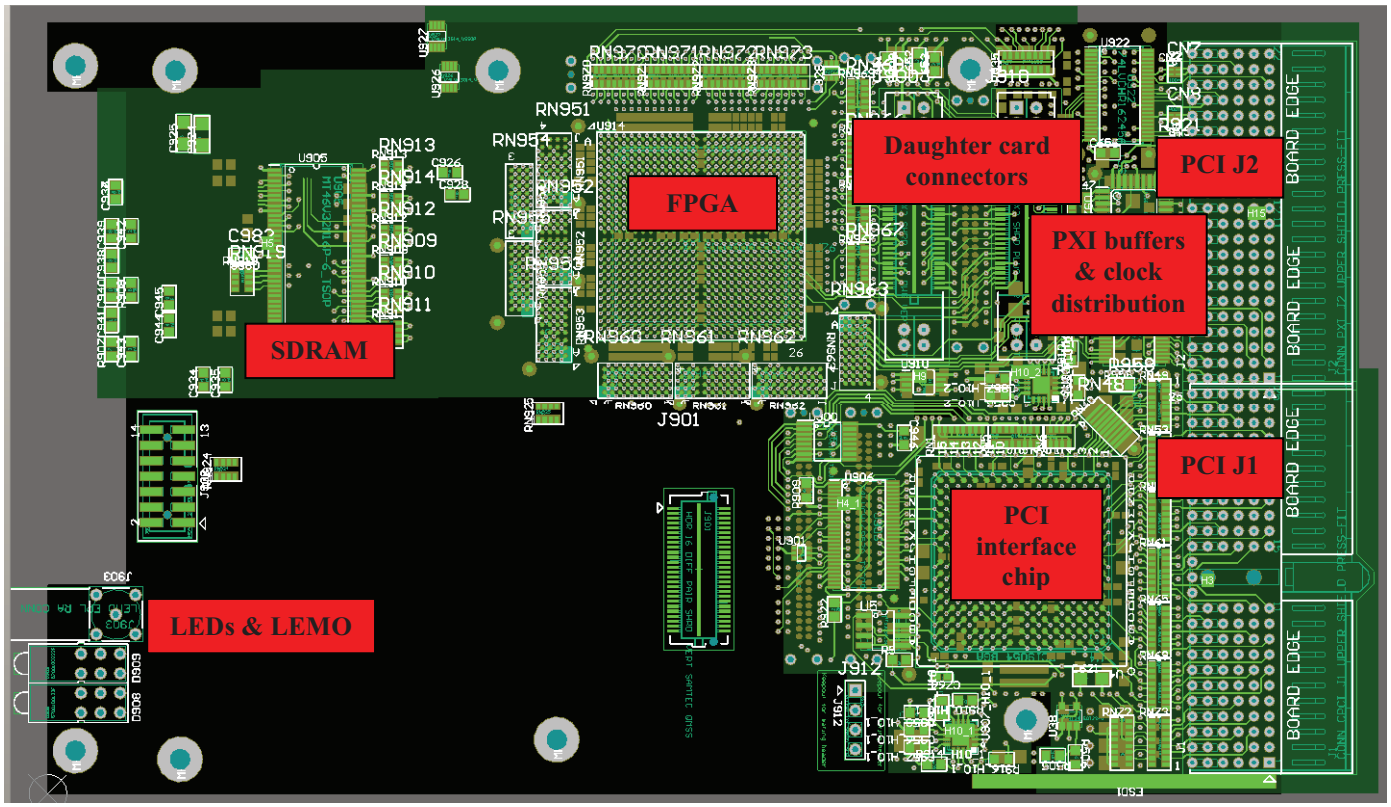

Fig. 2. 2D view of the core processor board.

III. Core Processor Board

Fig. 2 shows the 2D view of the core processor board in a CAD design environment. The 3U core processor board, equipped with PCI connectors J1 and J2, operates in a standard 3U cPCI/PXI crate. A daughter card is mounted to the top surface of the core processor board through the core-to-daughter connectors, forming a core-daughter combination board that only occupies a single slot of the crate. The core processor board and daughter card share one front panel where two sets of LEDs and one LEMO logic signal connector are also present. The central component of the core processor board is the FPGA (Xilinx Spartan-3A DSP) which processes the multiplexed data stream from the daughter card, accumulates MCA spectra for each channel, interfaces to external chips (SDRAM, PCI interface), and synchronizes data acquisition with other core processor boards in the crate.

The core processor board supports the following operation modes. The first mode is the MCA histogram mode. This is the main operation mode in which MCA energy histograms are accumulated for each channel (or detector pixel). Run statistics, e.g., run time, input count rate, output count rate, etc., are counted and computed for each channel as well. The second mode is list mode in which the computed pulse height (energy) and timestamp of the detected events are stored in the on-board memory (SDRAM) on the event-by-event basis. The third mode is the diagnostic mode in which a user can continuously stream the waveform data from selected channels and save

the data to the hard drive of a host computer for offline processing. This mode is useful for checking the status of health of the detectors or for refining the parameters for on-board signal processing.

Data is transferred between the core processor board and a host computer through the PCI interface chip on each core processor board, the PCI bus on the backplane of a crate, and a PCI bridge link between the crate and the computer. Data acquisition and board clocks can be synchronized between core processor boards through bus lines on the backplane of the crate.

IV. Daughter Card Example

We demonstrate here a daughter card as an example, i.e., the option A daughter card which accepts signals from microcalorimeters with individual analog outputs. Other daughter cards have very similar digital sections (format PFGA, connectors to core processor board, etc.), but they have different analog sections and front panel connectors. The Option A daughter card is an 8-channel board with 8 SMB connectors located on its front panel. Input signals will first be adjusted for their DC offsets using the on-board Offset DACs and then passed through anti-alias filters before being digitized by the 16-bit 1 MHz ADCs (ADS8329 from Texas Instruments). This ADC uses an external reference with a range from 0.3 V to 5.0 V. Therefore, by adjusting the external reference, one can change the effective gain of the analog inputs at the digitization stage.

The daughter card interfaces to the core processor board through three connectors: one power connector and two signal connectors. The daughter card receives ± 12 V, 3.3 V and 1.2 V from the core processor board and makes the following voltages locally: ± 6.5 V and 5 V. The 16-bit, 8 MHz data stream created by the format FPGA is sent to the core processor board through the signal connectors; clock, FPGA programming and other control signals are also passed through the same connectors.

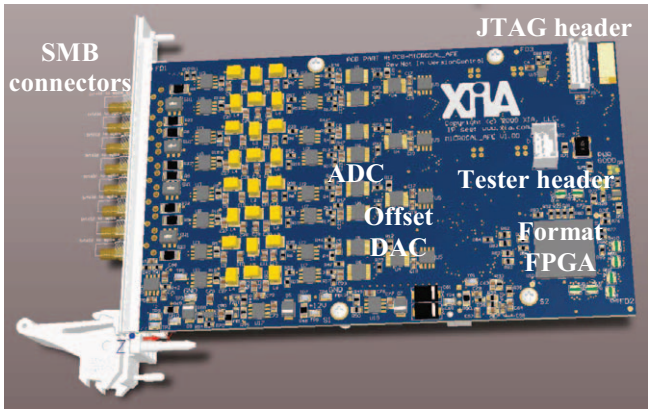

Fig. 3. 3D top view of the analog inputs daughter card.

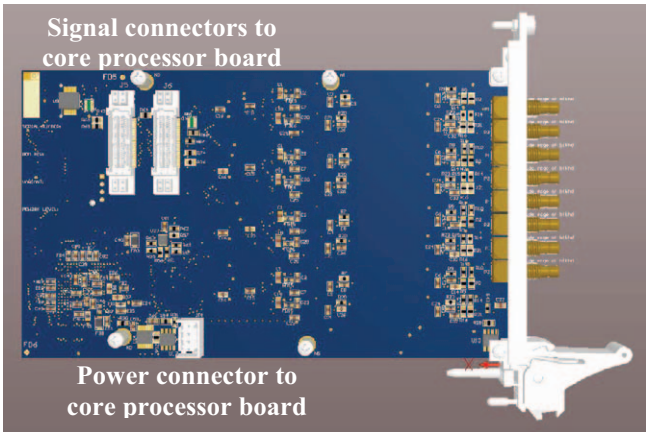

Fig. 4. 3D bottom view of the analog inputs daughter card.

V. Conclusions

The prototypes of the core processor board and the analog inputs daughter card are now close to production. Once we possess the prototypes, we will first characterize the performance of the daughter card and core processor board, and then we will make measurements with these prototypes in our collaborating institutes or laboratories (e.g., LANL/NIST, LLNL/LBL, Harvard, etc.). We are also designing and making the other two types of daughter cards. The final hardware will be made once the tests on the prototypes are completed.

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