Data Acquisition and Trigger System of the Gamma Ray Energy Tracking In-Beam Nuclear Array (GRETINA)

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***Abstract*—The Gamma Ray Energy Tracking In-Beam Nuclear Array (GRETINA), capable of determining the energy and position (within 2 mm) of each gamma-ray interaction point and tracking multiple gamma-ray interactions, has been designed. GRETINA will be composed of seven detector modules, each with four highly pure germanium crystals. Each crystal has 36 segments and one central contact instrumented by charge sensitive amplifiers. Two custom designed modules, the Digitizer/Digital Signal Processing (DSP) and the Trigger Timing and Control, compose the electronics of this system. The Digitizer/DSP converts the analog information with 14-bit analog to digital converters (operating at 100 MS/s, and digitally processes the data to determine the energy and timing information of the gamma interactions with the crystal. Each Digitizer/DSP is controlled by and sends trigger information to the Trigger Timing & Control system through a bidirectional Gbit link. Presently four different trigger algorithms are planned for the trigger system and can be selected for trigger decision. In this paper the details of the electronics and algorithms of the GRETINA data acquisition and trigger system are presented and the performance is reviewed.**

***Index Terms*—Data acquisition systems, digital signal processing, gamma-ray spectrometer, trigger systems.**

I. Introduction

WE have designed a data acquisition and trigger system for the Gamma Ray Energy Tracking In-Beam Nuclear Array (GRETINA). GRETINA is based on germanium detectors and it will be capable of determining the energy and position (within 2 mm) of the points of interaction of the gamma-rays with the germanium crystal and of tracking multiple gamma-ray interactions [1], [2]. GRETINA is composed of seven detector modules, each with four high purity germanium crystals (see Fig. 1), comprising a quarter or 1-π of a sphere. The detector module components include charge sensitive amplifiers [3] assembled inside the detector enclosure to instrument each of the 36 segments and the central contact. The gamma ray interaction with the germanium crystal induces charge on the segments and central contact. The amplifiers integrate this charge and drive an analog voltage to the GRETINA front-end electronics.

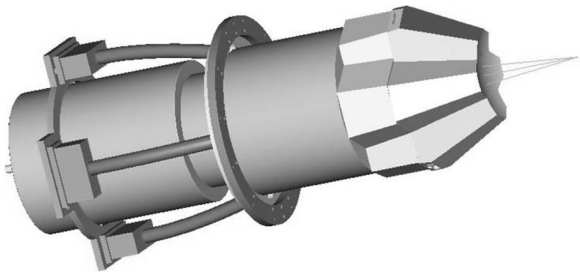

Fig. 1. GRETINA detector module.

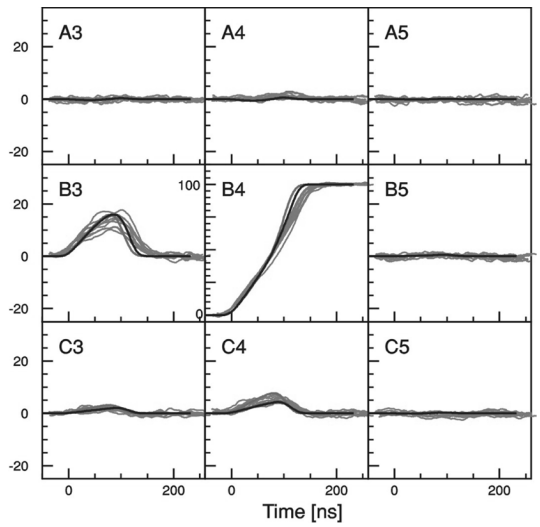

Fig. 2. Waveforms for interactions below segment B4.

For illustration, Fig. 2 shows examples of typical waveforms on the output of the amplifiers. The gamma-rays from a collimated ^{137}Cs source are interacting with the detector at a specific location below the B4 segment. The segments shown are the one that collects the charge (B4) and its eight nearest neighbor segments. The neighbor segments detect induced charge. A total of 16 measured shapes are plotted in gray and calculated signals at this given position are plotted in black; the agreement between calculation and measurement is very good. Observe that the measured signals include noise.

The detector modules are supported by a mechanical structure composed of two quasi-hemispheres shells that surround

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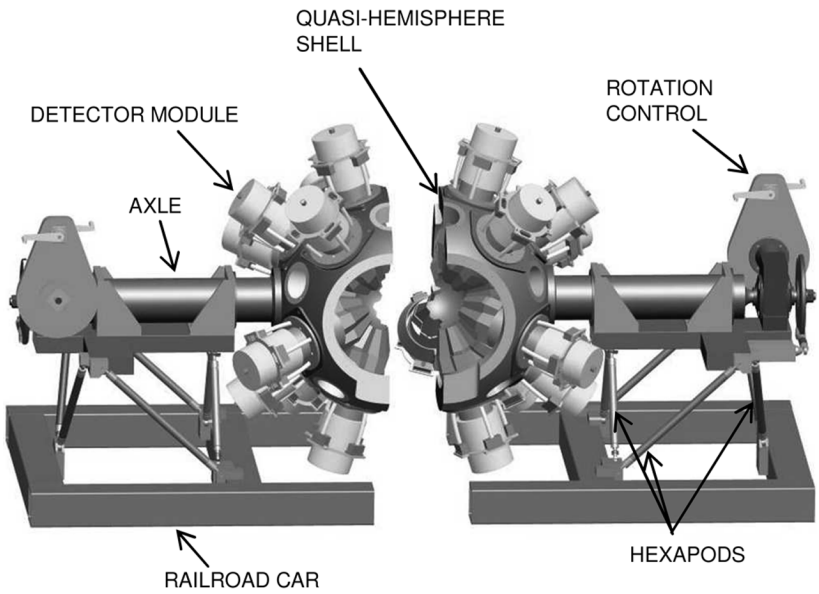

Fig. 3. GRETINA mechanical support structure.

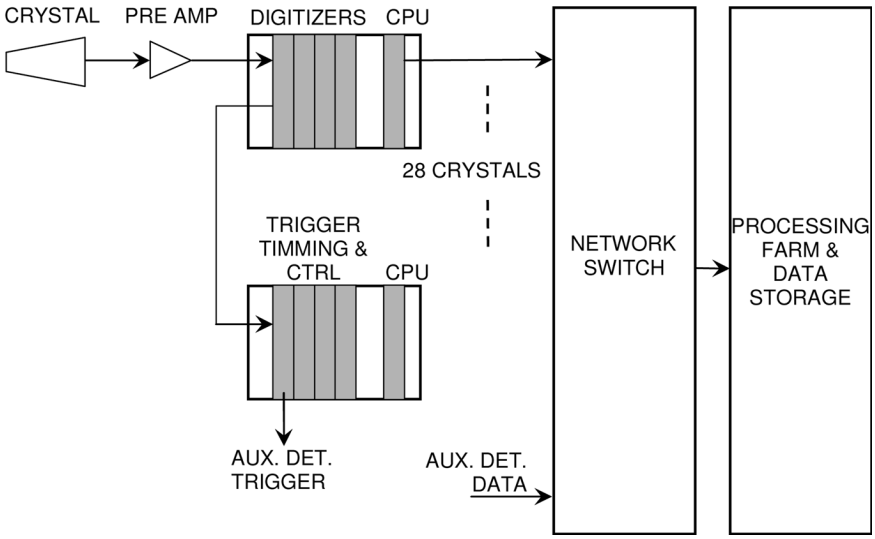

Fig. 4. GRETINA electronics and computing systems.

the target chamber. This shell structure is capable of supporting 21 detector modules. The structure allows rotation for detector mounting (through a gear box in the end of the axles) and translation to access the target chamber (through railroad cars). Hexapods connect the structure to the railroad cars. Fig. 3 shows a sketch of the support structure, with all possible positions instrumented with a detector module. There are plans to construct the full 4-π detector module array, GRETA [4], and the electronics system foresees this possible scenario.

In this paper the details of the electronics and algorithms of the GRETINA data acquisition and trigger system will be presented and the performance will be reviewed. In addition, grounding and filtering techniques used to achieve the 14-bit analog to digital conversion (ADC) performance will be discussed, as well as transmission line techniques for the very low bit error rate of the gigabit links.

II. System Architecture

Fig. 4 shows a block diagram of the GRETINA Electronics and Computing Systems. The oblong shape on the left represents the detector modules and its crystals. Charge sensitive amplifiers instrument the segments and central contact. Fifteen meters of shielded twisted pair cable connect the pre-amplifier outputs to the digitizer modules. Two custom designed modules, the Digitizer/Digital Signal Processing (Digitizer/DSP) and the Trigger Timing & Control (TTC), compose the electronics of this system. Four Digitizer/DSP modules instrument one crystal: each master Digitizer/DSP interfaces with the TTC system and controls three slave Digitizer/DSP modules. A digital bus in the front panel allows the digitizers serving a crystal to synchronize among themselves for clock and trigger information. A very simple communication protocol based on a single master controlling the operations is used.

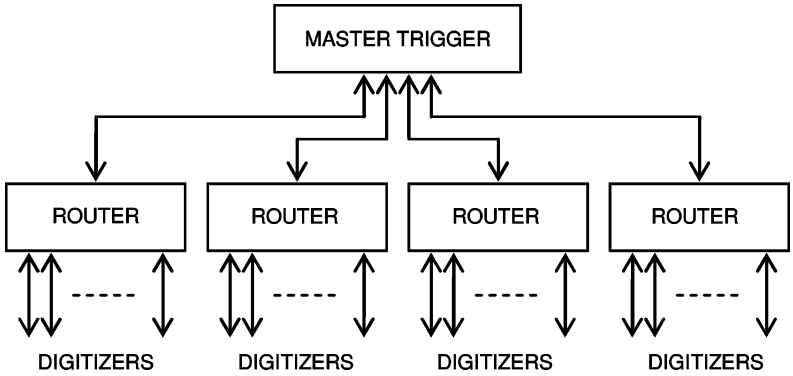

Fig. 5. TTC router and master connection.

The master digitizer monitors the crystal central contact. If a gamma ray deposits charge in the crystal above the programmable threshold of the leading edge (LE) discriminator, the master Digitizer/DSP recognizes the event and reads the segment hit pattern using the front panel bus. In parallel the Master digitizer estimates the energy of the central contact signal using a fast algorithm. It then assembles the trigger information (time stamp (TS) of the LE discriminator, central contact energy and segment hit pattern) and sends it to the TTC over one pair of a bidirectional 1 Gb/s serial link. A buffer records the timestamps of all recent discriminator decisions.

The serial link connecting the TTC and Digitizer/DSP modules is implemented using the National Semiconductor DS92LV18 Serializer/Deserializer (SerDes). It transmits 20 bits per word at a 50 MHz rate, where 18 bits are available for trigger and control information. The link meets the stability requirement of the system and has a predictable latency. The predictable latency allows the same twisted pair to transmit control information and provide the 50 MHz master clock to each Digitizer/DSP. The trigger information exchange between the master trigger and Digitizer/DSP employs a synchronous protocol and the master trigger module determines the synchronism. A synchronous implementation is easier to implement and maintain. The protocol consists of an endlessly repeating series of 20 command frames transmitted every 2 μs that allows the TTC system to regularly synchronize and control activities at the Digitizer/DSPs. Also, all trigger information from the Digitizer/DSP is transmitted to the TTC within this 2 μs window. The reason for a 2 μs period is to accommodate instantaneous fluctuations on the maximum average of one gamma interaction per crystal every 20 μs.

The whole TTC system is assembled around the same hardware module. The firmware is configured for two different functions: the Router module and the Master TTC. The Router routes all information between the Master TTC and the Digitizer/DSP modules and assists in fast multiplicity trigger decisions. The Master TTC collects all messages from the Routers plus additional information from auxiliary trigger modules and uses it to make a global trigger decision (refer to Fig. 5). Once a global trigger decision is made, the TTC system sends a trigger decision command to the Routers for distribution to all master Digitizer/DSP modules and auxiliary detectors. Each master Digitizer/DSP identifies a match between the timestamp embedded within the trigger decision message and the saved LE discriminator timestamps, and requests all slave Digitizer/DSP to transfer the data from the circular buffer into its own readout FIFO. Later, the VME readout CPUs in the digitizer crates read the event data from each Digitizer/DSP FIFO, assemble the crystal event, and send the data to the network switch. The switch routes the events to the computing farm where they are processed. The processing uses the segment information to estimate the position (r, θ, z) and energy of the interaction points. Additional processing establishes the tracks by connecting the individual interaction points.

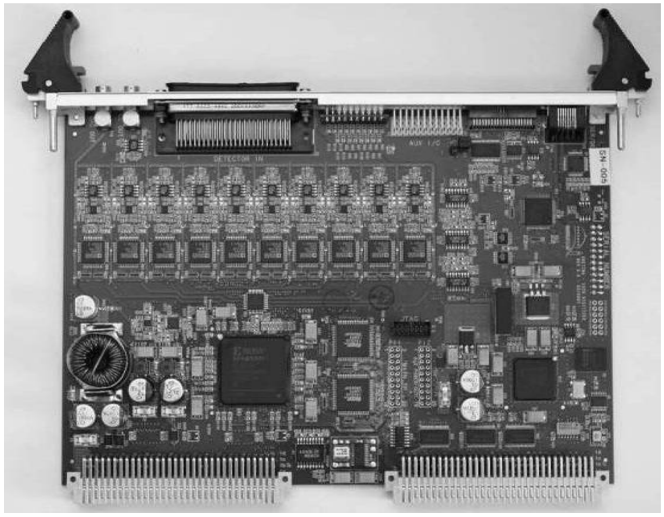

Fig. 6. Digitizer/DSP module.

We have extensively tested the performance of the DS92LV18 SerDes for bit error rate (BER). We have run 12 SerDes links in parallel for more than 10 consecutive days with no errors, which corresponds to a BER better than 10^{-16} or less than one error per day for GRETINA (four per day for GRETA). This component is a very simple SerDes that adds minimum protocol (an important characteristic for the constant latency). In order to guarantee the DC balancing of the communication we encoded the data stream in the FPGA. This encoding operates in the following way. First, before sending a word, the FPGA sums the number of zero and one bits in the word. Then it determines the DC balance of the line due to previous transmissions (i.e., if it has sent more zero bits or more one bits). Finally, to keep

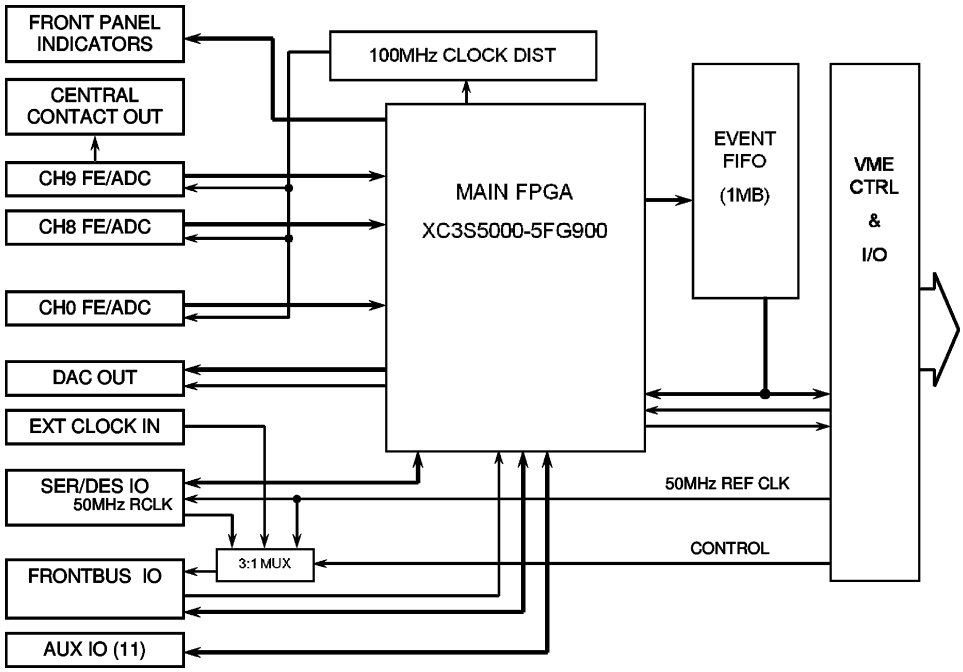

Fig. 7. Digitizer/DSP block diagram.

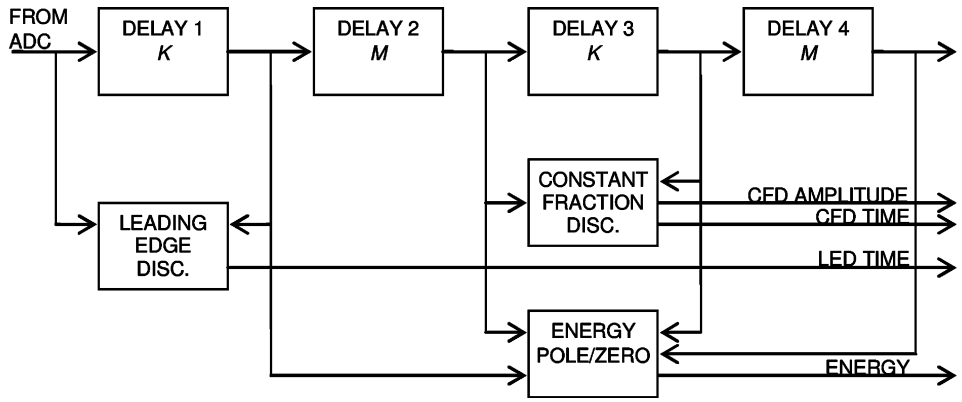

Fig. 8. Digital signal processing.

the line balanced, it then transmits the word itself or its complement. A dedicated bit in the word is set or reset to indicate to the receiver how to decode it. Also, we observed that replacing the cable from unshielded CAT5 to a good quality shielded CAT5 decreased the BER to the level reported above. LVDS drivers (DS90LV004) with programmable pre-emphasis are used in all modules to compensate for cable losses.

Each Digitizer/DSP and TTC module is implemented using two field programmable gate arrays (FPGA): one is a smaller FPGA, which controls the VME interface and has a steady configuration, and the other is a larger FPGA which executes the module specific algorithms and is easily re-configured through VME.

III. Digitizer/DSP

The Digitizer/DSP module samples the crystal segment and central contact analog information using 14-bit ADC operating at 100 MS/s. The ADC used is the AD6645 from Analog Devices. Fig. 6 shows a picture of the module and Fig. 7 shows its block diagram. The Digitizer/DSP has a total of 10 analog inputs. The ADCs are connected to an FPGA, which digitally processes the conversion and executes the following operations: leading and constant fraction discrimination, trapezoidal filtering, energy determination, and pole/zero cancellation.

Fig. 8 shows a block diagram of the digital processing algorithms and how they interconnect and Table I describes the algorithms. The processing is optimized to be implemented using the internal FPGA resources and occurs at a clock rate of 100 MHz, which is generated inside the FPGA by multiplying the 50 MHz master clock distributed from the TTC. This results in approximately 20 giga-operations/s. While the processing occurs, the raw data is stored in 40 μsec circular buffers (designed around the FPGA block RAMs). For further details about these algorithms refer to [5].

The present noise performance of the ADC inputs at full digital processing rate is approximately 1.5 RMS counts for all inputs (refer to Fig. 9). Achieving this performance in a board with digital power supplies and heavy digital activity required special

TABLE I
DIGITAL SIGNAL PROCESSING

Leading Edge Discrimination
$y(n)=x(n)-x(n-k)$ (differentiation)
$y(n)=(x(n)+x(n-2))+x(n-1)<<1$ (×4, Gaussian filtering)
Threshold comparison → LE discriminator time
Constant Fraction Discrimination
$y(n)=x(n)-x(n-k)$ (differentiation)
$y(n)=(x(n)+x(n-2))+x(n-1)<<1$ (×2, Gaussian filtering)
$y(n)=x(n-k)<<ab-x(n)$ (constant fraction)
Zero crossing comparison → CFD time
Trapezoidal filter and energy determination [6]
$y(n)=y(n-1)+((x(n)+x(n-2m-k))-(x(n-m)+x(n-m-k))$
Maximum tracking → energy
Pole-Zero cancellation
$I(n)=I(n-1)+x(n)$
$y(n)=x(n)+I(n)/t$ (where t is the pre-amp time constant)

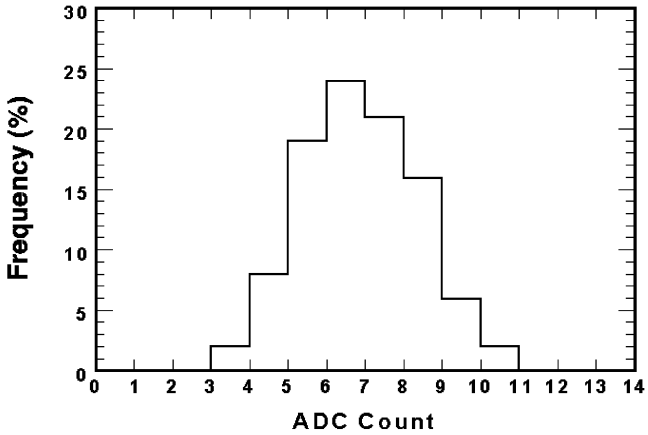

Fig. 9. Noise distribution: $\sigma = 1.5$ counts.

attention. We have filtered the $+5$ V with a π-filter (observe the inductor on the left portion of Fig. 6). Also, the analog inputs are all implemented using balanced differential techniques.

During prototyping we found two sources of noise due to board layout: one associated with a stray capacitance and the other with the analog and digital ground separation. For the first source we measured about 15 RMS counts and we observed that the ADC noise spectrum was not constant: it was mostly flat until ~ 15 MHz; then it increased by 6 dB/oct until ~ 30 MHz where it became mostly flat again. The increase at 15 MHz was traced to a stray capacitance between the input of the differential amplifier and the ground plane. This capacitance limited the amplifier feedback and, therefore, increasing the gain for higher frequencies (i.e., larger than ~ 15 MHz). At ~ 30 MHz the amplifier reached the maximum frequency response and the gain stabilized again. To reduce this stray capacitance we modified the layout and removed the ground plane right below the differential amplifier inputs. For the second source of noise we observed that the RMS noise performance was not similar for all ADC channels: the ADCs on the left portion of the board (i.e., close to the π-filter, refer to Fig. 6) had approximately 1.5 RMS counts while the ones on the right had approximately 3 RMS counts. We then changed the layout and cut the ground plane around the analog section to create an analog ground mostly free of digital switching. We connected the analog ground together with the digital ground under the ADCs (as suggested on the datasheet) and also close to the π-filter. With these two layout changes we now obtain approximately the same noise performance to all channels.

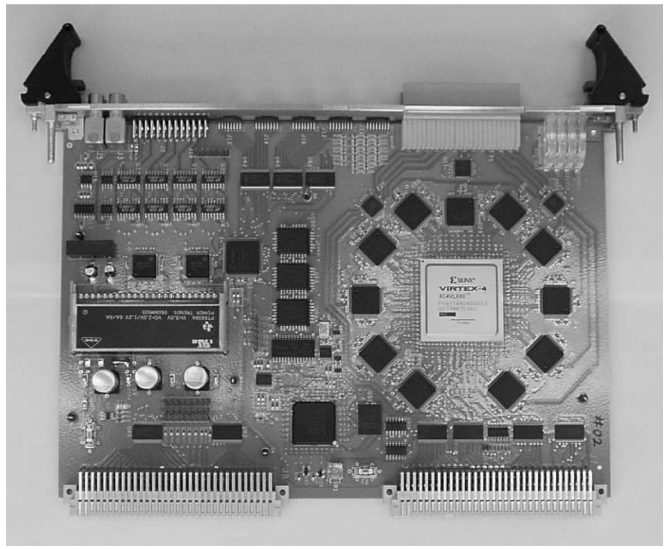

Fig. 10. Trigger, timing and control module.

The Digitizer/DSP module also has programmable digital inputs and outputs for interfacing with other units and front panel LE discriminators for status. All the processing described above is done in a XC3S5000 FPGA from Xilinx. Presently about 50% of the FPGA is utilized, allowing for further increase in algorithm complexity.

IV. TRIGGER, TIMING AND CONTROL

Fig. 10 and 11 show the picture and block diagram of the TTC module, respectively. The TTC is presently configured for multiplicity algorithm, and we intend to add three more in the next few months. When completed, the trigger algorithms will be:

a) *Multiplicity*: Uses the LE discriminator detection of the crystals central contacts. The TTC generates a trigger when it detected that the sum of LE discriminators crosses some threshold within a time window.
b) *Energy*: uses the energy of a central contact or the sum of energies of central contacts. When this energy falls within some programmable window the TCC generates a trigger.
c) *Pattern distribution*: It also uses central contact energy as described above. The TTC triggers when it detects coincidence of gamma-rays energy above threshold in any two pre-programmed crystals.
d) *Auxiliary detector trigger*: The TTC receives an external trigger within the 40 μsec pipeline depth of the Digitizer/DSP.

We call these algorithms prompt triggers, because a trigger is generated as soon as the proper condition is detected. A delayed coincidence trigger can further refine the meaning of these prompt triggers. When this option is enabled, the TTC generates a trigger command when it detects two prompt trigger conditions (e.g., two multiplicity triggers) in two time windows within the allowed overall trigger window. Finally, observe that all the trigger parameters are configurable through VME.

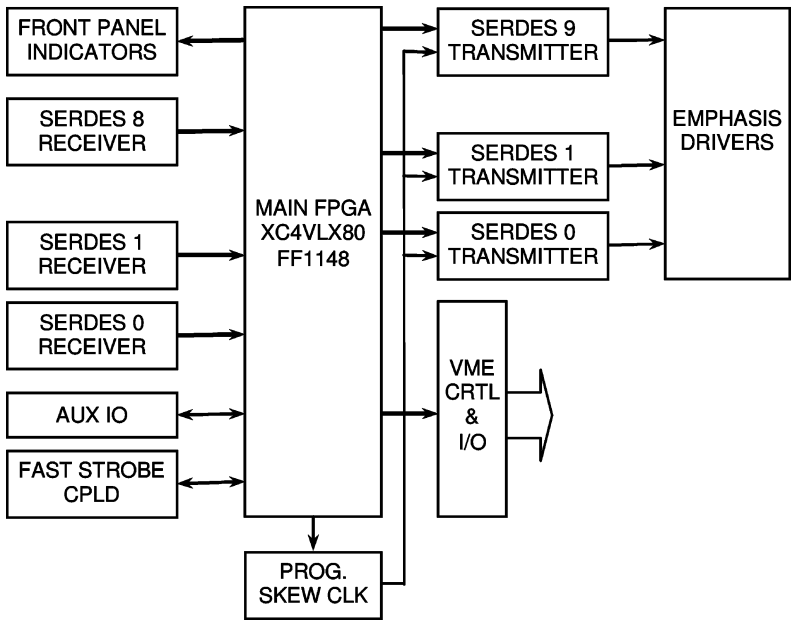

Fig. 11. Trigger, timing and control block diagram.

The main FPGA in the TTC module is the Virtex 4 series XC4VLX80 FPGA. This part executes the trigger algorithms and interfaces with eight SerDes. As already described, the SerDes components transfer information between the Digitizers/DSP. The base multiplicity algorithm presently uses only 15% of the resources inside this FPGA, which allows for further development of the trigger algorithms.

The high-speed switching of the SerDes has edge transition times in the order of 100 ps range. These high-speed signals require special attention during layout, and are more critical on the TTC (when compared with the Digitizer/DSP module), since it has eight SerDes and not all can be mounted close to the connector. Carefully matched, impedance controlled differential traces are used. Additionally, the number of vias was minimized: the component side transmits trigger information, and it does not have any vias, while the solder side is used to receive trigger information, and it has just one via per trace of the differential signal. To further improve signal fidelity, a mixed stackup is used where the dielectric under the component and solder layers of the board is Rogers 4350, which has lower losses than FR4.

The electronics requirements [7] state that the Digitizers/DSPs shall sample all crystals within a 2 ns clock phase window. To synchronize all these modules, all CAT5 cables between the TTC and the Digitizer/DSP are approximately of the same length. However, small cable and component delay differences may generate delays that exceed this limit. To compensate for small delay variations and allow field tuning without recompiling the FPGA firmware, the TTC uses programmable skew clock buffers (Cypress Semiconductor CY7B992) to adjust the delay of the transmit clock (TCLK) of each SerDes. This, in turn, changes the delay of the sampling clock of the Digitizer/DSP at the other end of the cable. To adjust the clock phases we intend to use an oscilloscope monitoring multiple clock outputs on the front bus of master digitizers followed by manual reconfiguration of the VME registers controlling the programmable skew clock buffers. Also, the system phase adjustment can be validated before, during and after an experiment by measuring coincidences between any pair of detectors using a radioactive ^{60}Co source that provides two gamma-rays in prompt coincidence.

GRETINA may provide trigger to auxiliary detectors. Some of these detectors use old technology and they do not have digital pipelines; the trigger decision has to be done when the signals are actually traveling on cables, and the sampling has to start when they arrived at the auxiliary electronics. Only the multiplicity algorithm will be used when interfacing with this type of auxiliary detectors. We have implemented a parallel path that by-passes the SerDes to meet the more stringent timing requirements. The SerDes add a delay of approximately 70 ns to serialize and de-serialize the data. This new path uses a dedicated available pair of the CAT5 cable to transmit from the Digitizer/DSP to the TTC system the status of the central contact LE discriminator detection. To determine multiplicity, the TTC makes the sum of the LE discriminators using front panel connectors and CPLDs. The partial sums travel from the Routers to the Master Trigger module, which executes the final sum and determines the multiplicity. We estimate that this processing will take less than 250 ns. Also, it is interesting to highlight that this requirement also imposed one of the criteria to select the ADC: the latency of the AD6645 is just three clock cycles, which allows for faster LE discriminator determination.

The TTC module also has programmable digital inputs and outputs for interfacing with other units (e.g., auxiliary detectors & NIM electronics) plus front panel LED for status.

V. Cable and Connector Selection

We have dedicated substantial effort in selecting the proper cabling for this electronics. One example already discussed is

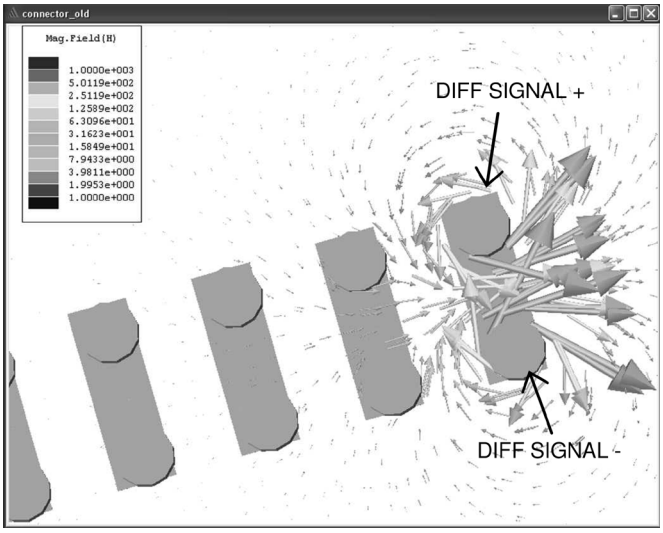

Fig. 12. Magnetic coupling in 0.1" spacing connectors.

the CAT5 cable for the SerDes. We will now describe the selection of another very important cable, the one that connects the detector pre-amplifiers to the Digitizers/DSPs, which carries the crystal interaction information. Reducing crosstalk between the signals in this interconnection is very important for estimating the position (r, θ, z) of the interactions points: excessive crosstalk decreases the position resolution of the gamma ray interaction. The requirement of total crosstalk in the detector module is less than 0.2% and, therefore, the rest of the electronics crosstalk has to be substantially less than this (required of $< 0.04\%$). To avoid ground loops we decided that the input of the Digitizers/DSPs would be differential and that we would employ twisted pairs. We tested several cables. We obtained the best performance with twisted individually shielded pairs. The crosstalk between adjacent pairs was $< 0.04\%$ for a 15 m cable span. For comparison, a similar cable, but non-twisted (used for LVDS transmission), had a crosstalk of $\sim 2.5\%$. This crosstalk is explained by the magnetic field created in one pair passing through the shielding and magnetically coupling to an adjacent pair. The shielding between pairs is a thin aluminum layer, and it does not attenuate the magnetic field significantly for these speeds. These tests considered a constant rise time (10%–90%) of 30 nsec, well within the expected rise times in GRETINA.

For the connector between the cable and the digitizer we have also tested several connector types, and we also observed crosstalk between signals. We traced the crosstalk, again, to the magnetic field of one signal coupling into the next signal. This can be visualized in Fig. 12. This figure shows the results of Maxwell simulations [from Ansoft] where the arrows represent the direction and the magnitude of the magnetic field. These simulations were done considering that the positive input of the differential signals are connected on the top row and the negative on the bottom row, forming these differential connections. The offending signal uses the differential connection on the right. One can observe that the magnetic field propagates well into the

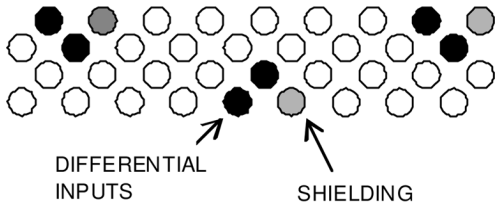

Fig. 13. IIT-Cannon connector pin assignment.

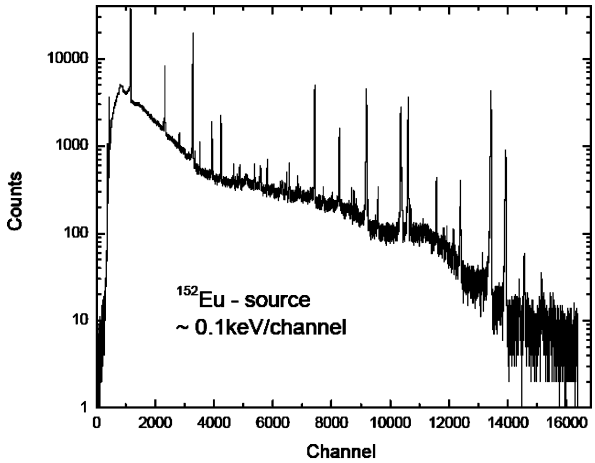

Fig. 14. Energy spectrum for a ^{152}Eu source.

adjacent differential connections, causing crosstalk. The connector simulated has 0.1" pin spacing. Ways to mitigate this effect are threefold: (a) increasing the distance between differential connections, (b) selecting the direction of the pairs (ideally in an angle of 90°), and (c) short circuiting unused connector pairs (to create an opposing magnetic field that decreasing the offending field). For example, the simulations and subsequent tests have demonstrated that skipping two differential connections (on the right of the offending differential connection) and using the third for the next signal decreased the crosstalk by $\sim 10\times$, and that short circuiting these two unused set of pins reduces the crosstalk on the third pair by a further $\sim 2.5\times$. These tests were run with a 100 MHz sinusoidal signal. To meet the crosstalk mitigation strategies outlined above we used a 100 pin Double Density, Subminiature D type connector manufactured by ITT-Cannon. Fig. 13 shows a sketch of how we connected the differential pairs (represented by back circles) and its individual shielding (represented by gray circles). The figure shows the sketch of just a portion of the connector. The unused pins were short circuited in pairs. With this arrangement the measured crosstalk was below what we can measure using 14-bits ADC of the Digitizer/DSP (i.e., crosstalk $< 0.025\%$). The signal used had a constant rise time (10–90%) of 30 nsec.

VI. Test Results and Conclusions

We have tested the performance of the DAQ and trigger system connected to a detector module and we will now describe a few results we have obtained. For these tests we used the production cables and floating low- and high-voltage (bias) supplies. Fig. 14 shows a ^{152}Eu source energy spectrum obtained with the central contact of one of the crystals.

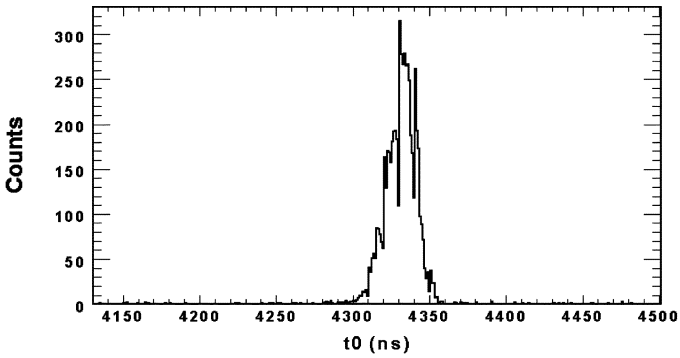

Fig. 15. Constant Fraction discriminator performance.

Fig. 2 shows waveforms that are similar to the waveforms the DSP/Digitizer module records. Fig. 15 shows a time spectrum used to measure the performance of the constant fraction discriminator in the digital processing. The T_{O}, derived from the FPGA algorithm is referenced to a very fast external trigger provided by a CsF scintillator with essentially no contribution to the width. The standard deviation of the Gaussian fit is 9 ns.

All tests with the prototype system indicate that the DAQ and Trigger systems for GRETINA will meet the requirements. We are presently preparing the production of the system to enter in operation in 2011.

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REFERENCES

[1] I. Y. Lee, "Gamma-ray tracking detectors," *Nucl. Instrum. Methods Phys. Res. A*, vol. A422, pp. 195–200, Feb. 1999.

[2] M. A. Deleplanque *et al.*, "GRETA: utilizing new concepts in γ-ray detection," *Nucl. Instrum. Methods Phys. Res. A*, vol. A430, pp. 292–310, Jul. 1999.

[3] F. S. Goulding and D. A. Landis, "Semiconductor detector spectrometer electronics," in *Nuclear Spectroscopy and Reactions Part A*, J. Cerny, Ed. New York: Academic, 1974, pp. 413–481.

[4] The Future of Gamma-Ray Spectroscopy: GRETA, the Gamma-Ray Energy Tracking, 2006 [Online]. Available: http://fsunuc.physics.fsu.edu/~gretina/GRETA_WP_Jan07_4.pdf

[5] M. Cromaz *et al.*, "A digital signal processing module for gamma-ray tracking detectors," *Nucl. Instrum. Methods Phys. Res. A*, vol. A597, pp. 233–237, Dec. 2008.

[6] V. T. Jordanov and G. F. Knoll, "Digital synthesis of pulse shapes in real time for high resolution radiation spectroscopy," *Nucl. Instrum. Methods Phys. Res. A*, vol. A345, pp. 337–345, Jun. 1994.

[7] F. Bieser, I.-Y. Lee, A. Macchiavelli, J. Weizeorick, and S. Zimmermann, GRETINA Electronics Requirement Document LBNL, Berkeley, 2005, Doc. GRT-3-041115.