Digital Data Acquisition Modules for Instrumenting Large Segmented Germanium Detector Arrays

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***Abstract*–XIA LLC has developed a 16-channel digital gamma-ray spectrometer (DGF Pixie-16) and associated electronics for instrumenting segmented germanium detector systems with large numbers of channels. The Pixie-16 is a CompactPCI/PXI-based data acquisition module equipped with 100 MHz 12-bit digitizers, signal processing field programmable gate arrays and a digital signal processor. Housed in a custom 6U PXI chassis, its operation can be extended to multiple chassis by using modules which distribute clock and triggers between chassis in LVDS format to achieve high speed and low distortion transmission. XIA LLC has collaborated with the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University in the construction of a fully Digital Data Acquisition System (DDAS) for instrumenting the 594-channel Segmented Germanium Array (SeGA) at NSCL. Using its gamma-ray tracking capability and consequently improved precision in determining gamma-ray interaction positions in the SeGA detectors, the DDAS will significantly improve their ability to determine gamma-ray emission angles and thus achieve better Doppler corrections. In this paper, we demonstrate the capability to achieve sub-nanosecond timing resolution when capturing waveforms in modules across multiple chassis in response to common global triggers. We then discuss the NSCL DDAS firmware solution, especially considering its capability for data acquisition with near zero dead times.**

I. INTRODUCTION

RECENT advances in digital electronics have allowed the instrumentation of large segmented germanium detector arrays to move from the traditional analog data acquisition systems to digital data acquisition systems. Compared to their analog counterpart, digital acquisition modules offer compactness, versatility, and most often cost-effectiveness. Furthermore, it is possible to capture and store waveforms on an event-by-event basis with the digital acquisition modules, and then perform identification of gamma-ray interaction positions in segmented germanium detectors from pulse shape analysis. Precise knowledge of the first interaction positions in the detectors improves the determination of the angle of emission of the gamma-rays and thus results in better Doppler corrections [1].

XIA LLC has developed a 16-channel digital gamma-ray spectrometer (DGF Pixie-16) [2], [3] and associated electronics for instrumenting a large number of channels of segmented germanium detector systems, and has collaborated with the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University in the construction of a fully Digital Data Acquisition System (DDAS) for instrumenting the 594-channel Segmented Germanium Array (SeGA) at NSCL. The SeGA DDAS must meet the following requirements: 1) instrumenting all 594 SeGA channels and possibly other auxiliary detectors; 2) capability to capture waveforms synchronously in all channels with a jitter of less than 1 ns in response to a common global trigger; 3) capability to process signals in real time at the rate of at least 1000 counts per second per SeGA detector; 4) capability to measure pulse height and accumulate Multichannel Analyzer (MCA) histograms in real time; 5) capability to generate triggers at both local and global levels; and 6) capability to work with other detectors (e.g. the S800 spectrograph at NSCL [4]).

The architecture of the DGF Pixie-16 had been previously reported [2], [3]. The method for distributing clocks and triggers between multiple PXI chassis containing Pixie-16 modules has also been demonstrated [2]. In this paper, we focus on the implementation of coincidence triggering and synchronous waveform acquisition in the firmware and software of the Pixie-16 for instrumenting the 594-channel SeGA array and demonstrate that it meets the above requirements. In particularly, we illustrate the NSCL DDAS' capability for data acquisition with near zero dead times.

II. DDAS SYSTEM IMPLEMENTATION

Fig. 1 is the NSCL DDAS diagram illustrating the instrumentation of 18 SeGA detectors and other auxiliary detectors in four 14-slot 6U PXI chassis. Each chassis is controlled through a fiber optical PCI Bridge to a computer running the Linux operating system. There are a total of 39 Pixie-16 modules installed in the DDAS, 3 (two "Assistants" and one "Director") in the first chassis and 12 (in "Manager"/"Worker" pairs) in each of the three other chassis. Each Manager/Worker pair (32 total channels) instruments one SeGA detector. The central contacts of the 18 SeGA detectors are split into two groups of 9, and each group is connected to either the left or right Assistant module in the first chassis. The Director makes the trigger decision based on

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the fast triggers from the Assistants (e.g. event multiplicity) and an external validation trigger from auxiliary detectors, and then sends the trigger decision to the Assistants and Manager/Worker pairs for them to record the event. Event data recorded in the Pixie-16 modules are read out to the host computer through the PCI Bridge which can reach sustained read-out speeds of approximately 80 MByte/second.

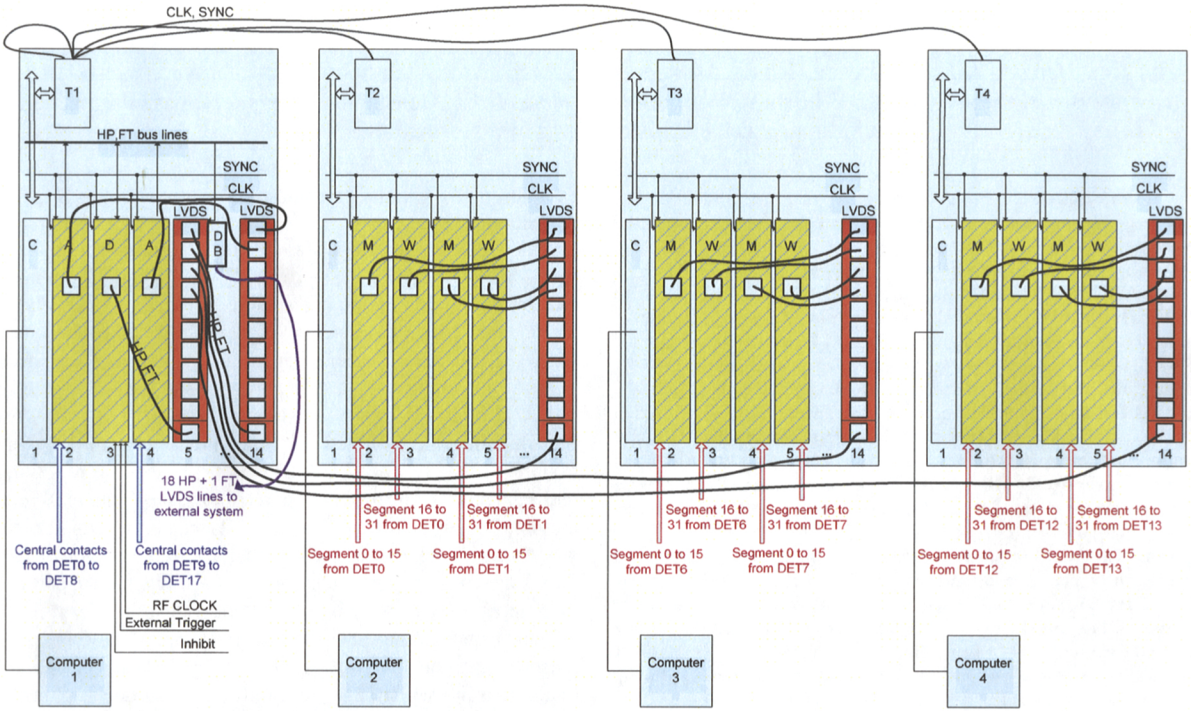

Fig. 1. The NSCL DDAS diagram.

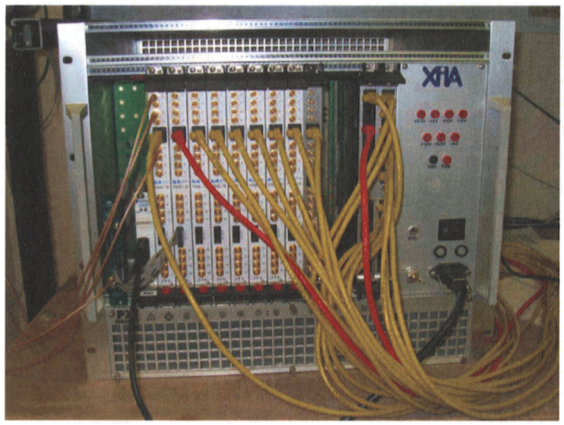

Fig. 2. Pixie-16 chassis.

Fig. 2 shows one Pixie-16 PXI chassis in which multiple Pixie-16 modules and trigger distribution LVDS fanout modules are installed. On the far left of the chassis is a small adapter board which connects signals such as external trigger, RF clock and run inhibit to the Director module's front panel digital I/O port. Next to the adapter board is the PXI/PCI bridge card which connects the chassis to the host computer. Below we describe the implementation of clock and trigger distribution, synchronization, and zero dead time data acquisition.

A. Clock and trigger distribution

Clock pulses are distributed within a chassis through the PXI backplane and between chassis through rear I/O modules connected by equal length CAT-6 Ethernet cables [2]. The event hit pattern (HP) and global fast trigger (FT) are transmitted from the Director to all other modules using the Pixie-16's front panel 4-line LVDS port (which can be configured as either input or output), LVDS fanout modules installed in each chassis, and equal length CAT-6 cables. Each LVDS fanout module has one input and ten identical outputs. The first LVDS fanout module in the first chassis accepts the HP and FT from the Director and makes ten identical copies, four of them being sent to the four LVDS fanout modules installed in the last slot of each chassis. Each of those four fanout modules then makes 10 identical copies of the HP and FT, for a total of 40 copies. Each of the 38 Pixie-16 modules receives one copy of the HP and FT, excepting the Director, which is the source of HP and FT. Differences in propagation delays from clock source or Director to each module and each chassis (including itself) are thus ensured to be below 1 ns.

HP and FT can also be distributed to external systems for making global trigger decisions by using the LVDS Daughter

Board mounted on the LVDS fanout module. That external trigger can then be fed back to the Director through its front panel digital I/O port, either in TTL or LVDS format.

The Director can also count an external clock signal by accepting it through its front panel digital I/O port, and append this external clock timestamp to the event output data. This is useful for correlating events recorded simultaneously in two different systems, e.g. the DDAS and another data acquisition system which counts the same external clock signal.

B. Synchronization

Synchronization pulses are also distributed within a chassis through the PXI backplane and between chassis through the same CAT-6 cables as used by the clock distribution. Clock counters in each Pixie-16 module's FPGAs are reset to zero simultaneously when receiving the synchronization pulse at the start of a data acquisition run, thus ensuring common timestamps for the recorded events from all channels.

Data acquisition will also be started and stopped exactly at the same time in all Pixie-16 modules by using the synchronization pulses even though each chassis is controlled by a different computer. When starting a data acquisition run, host control software in each computer issues a "run start" command, but there may be delays between commands from different computers. To accommodate delays, a Pixie-16 module will not start its data acquisition until it sees a synchronization pulse on the backplane, which will only arrive when all Pixie-16 modules are ready for data acquisition. In the same way, when a host computer wants to stop the run, its "end run" command will be broadcasted to all chassis and modules simultaneously through the synchronization bus line, and all modules will stop their data acquisition at exactly the same time.

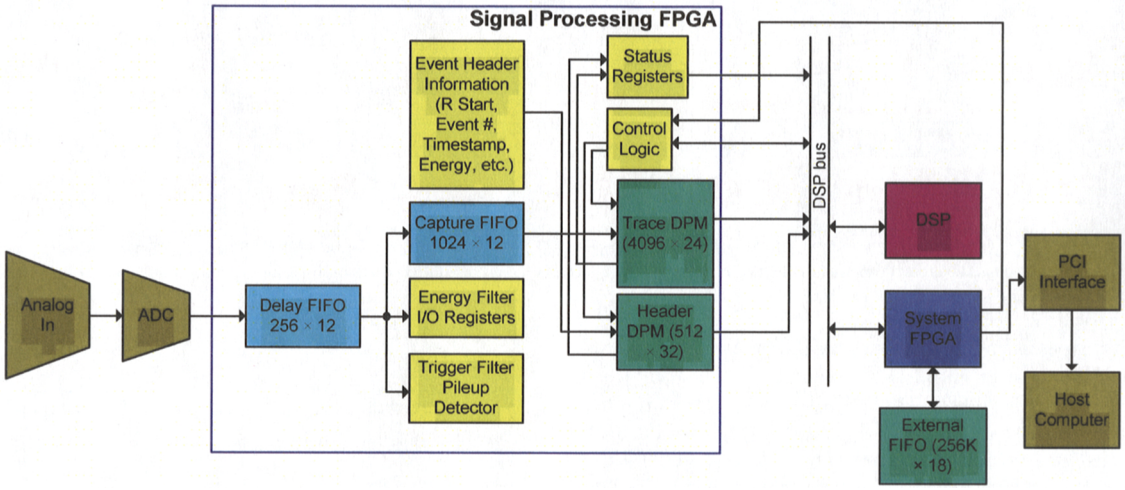

Fig. 3. Signal flow in the Pixie-16 module.

C. Implementation of zero dead time data acquisition

To achieve the lowest dead time during data acquisition, the DDAS uses two levels of data buffering, one in the signal processing FPGA and one in the list mode data External FIFO. Fig. 3 shows the simplified block diagram of Pixie-16 (only one signal processing channel is shown) and illustrates how the data flows through different parts of the Pixie-16 module. Two dual port memory blocks are used: one for storing waveforms and one for event headers (e.g. event number, timestamp, energy, etc.). For a typical waveform length of 2 μs, the Trace DPM will be able to buffer 40 waveforms. Waveforms and headers are then transferred through the System FPGA to the External FIFO, which can buffer approximately 74 events if each of the 16 channels records 2 μs waveforms plus an 11-word (32-bit) header per event. Therefore, as long as the host computer can read out data in the External FIFO fast enough so that data buffered in the Trace and Header DPMs can be streamed into the External FIFO without interruption, there will be no dead time caused by the data transfer. Since the sustained PCI readout rate can reach approximately 80 MByte/second, the system can achieve an output count rate of almost 1000 counts/second per SeGA detector without incurring readout dead time (at 1000 counts/s, the data rate is approximately 6.8 MByte/second per Pixie-16 module and 81.6 MByte/second for 12 Pixie-16 modules installed in one chassis).

III. Results and Discussion

The NSCL DDAS has been tested with both radioactive sources and in-beam experiments for its synchronous waveform capture capability, energy resolution, sub-nanosecond data acquisition jitter, and near zero dead time data acquisition.

Fig. 4 shows the sample synchronous waveforms captured from a single SeGA detector. The bottom axis of each of the

33 graphs is time in 10 ns clock ticks, and the vertical axis is ADC value in 12-bit ADC steps. The top graph is the waveform recorded for the central core of the detector, and the remaining 32 waveforms are captured from the detector's 32 segments. Among them, segment #14 and 15 share the deposited charge, and segment #2, 6, 7, 10, 11, 18, 19 and 22 shows induced charges, whereas all other segments do not exhibit collection of deposited or induced charge. Pulse shape analysis can be therefore performed on the acquired waveforms to determine the precise gamma-ray interaction position in the SeGA detector.

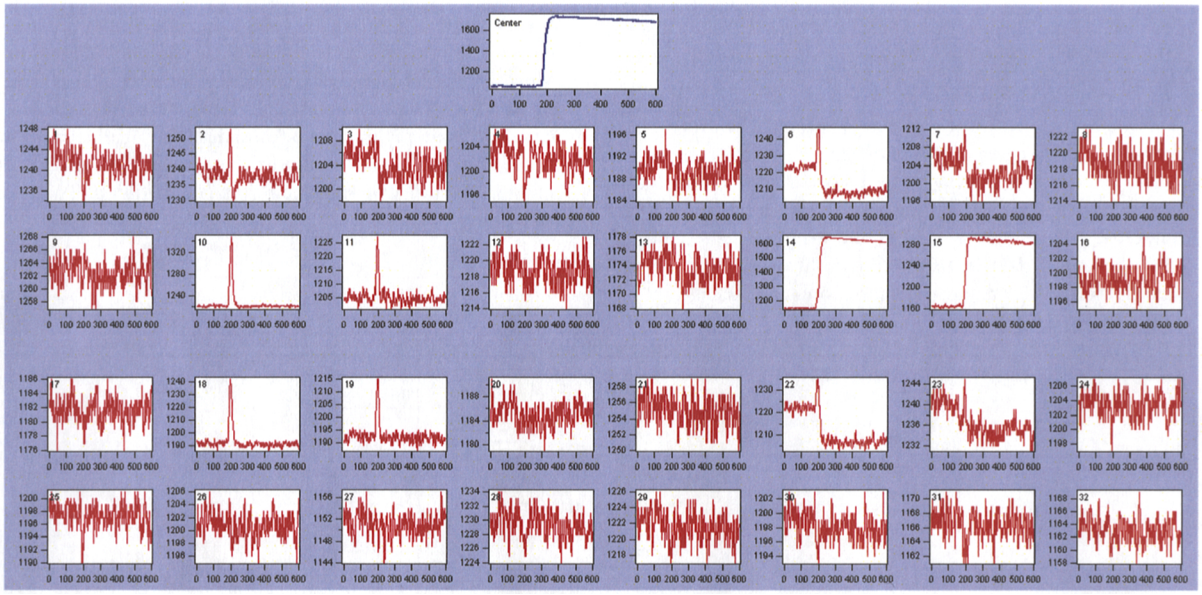

Fig. 4. Synchronous waveforms captured in one SeGA detector. The top one is the waveform recorded for the central core, and the other 32 waveforms are from the 32 segments.

Two types of energy resolution tests were carried out for the Pixie-16: one with XIA LLC's in-house 40% coaxial HPGe detector and the other with NSCL's SeGA detector. Their results are shown in Fig. 5 and 6, respectively. Both demonstrate excellent energy resolutions. A 1.75 keV FWHM at the 1332.5 keV line of ^{60}Co was achieved with the 40% coaxial detector, and clear separation of the 31.5 keV and 36 keV of the K_α x-rays from ^{137}Ba was shown with the SeGA detector.

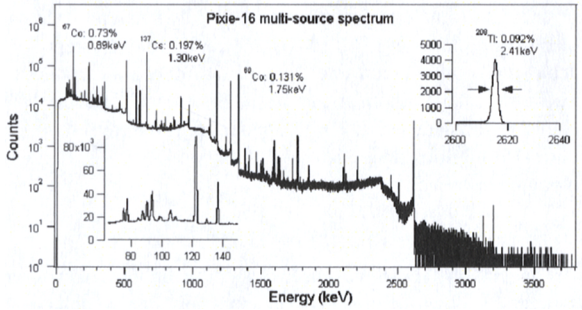

Fig. 5. Pixie-16 spectrum taken with multiple radioactive sources using an in-house HPGe detector at XIA LLC.

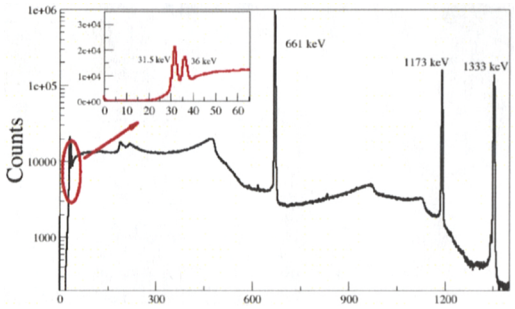

Fig. 6. Pixie-16 spectrum taken with multiple radioactive sources using a single SeGA detector at NSCL.

Fig. 7 shows the acquisition skew between two Manager/Worker pairs in one chassis. Pairs 1 (first pair) and 6 (last pair) are the two modules in Slot 2 and 3 and Slot 12 and 13, respectively. The acquisition skew was measured by first fitting sine waveforms acquired with a common trigger in each module pair, computing the phase shift between them, and histogramming results from thousands of waveforms to obtain a time-difference spectrum. The acquisition skew (peak width) is clearly in the sub-nanosecond range. Propagation delays cause an offset (peak position not at zero), but the offset is constant during measurements and can be calibrated out.

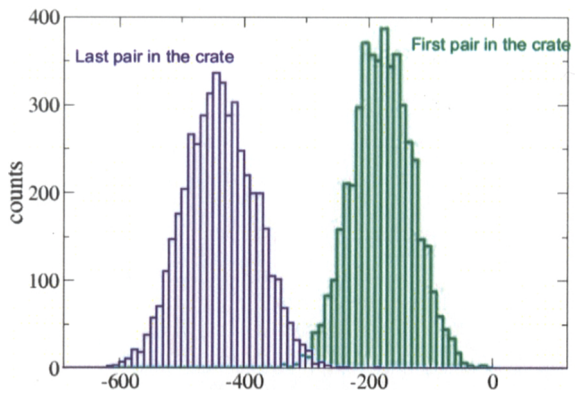

Fig. 7. Acquisition skew between manager/worker pair modules in one chassis.

To demonstrate zero dead time data acquisition, timestamp difference between subsequent events is calculated and histogrammed. A sample histogram is shown in Fig. 8. Events are nearly uniformly distributed for timestamp differences from 200 μs down to approximately 6 μs. The histogram then has a sharp cut off at about 6 μs, which corresponds to the pileup inspection period associated with the digital trapezoidal filter implemented in the Pixie-16. Therefore, there is no any additional dead time due to the data transfer from the FPGAs and FIFOs on the Pixie-16 to the host computer.

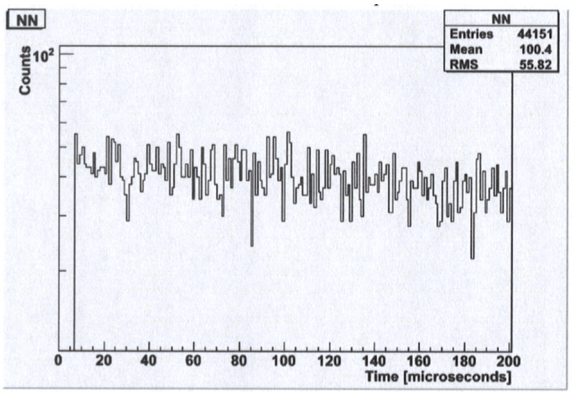

Fig. 8. Histogram of timestamp difference between subsequent events in a single SeGA detector.

IV. Conclusions

In summary, we have developed a digital data acquisition system, based on the DGF Pixie-16, for instrumenting the NSCL 594-channel SeGA detector system. These modules have been demonstrated to achieve synchronous waveform capture from all 594 channels, excellent energy resolution, sub-nanosecond data acquisition jitters, and near zero dead time data acquisition. The modules can be easily applied to other segmented germanium detector arrays by simply modifying the on-board firmware to suit the needs of different experiments.

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