Design of Front-End Electronic Circuits for Dedicated PET Detectors

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***Abstract*--The new high spatial resolution PET detectors for small animal and breast imaging have been designed. Position-sensitive photo-multipliers (R7600-C12) and dual-layer pixelated BGO crystals are employed to detect and localize gamma rays. A modified high-voltage divider with last dynode readout circuits, a front-end positioning readout circuits, and a last dynode timing amplifier have been investigated and developed for these detectors. Methods for combining four PS-PMTs with simple X–, X+, Y–, and Y+ outputs have been developed to further simplify the positioning processing. The front-end circuits are small so they can be fit in the detector's structure. A prototype of two detector modules, each having two PS-PMTs with corresponding electronic circuits, has been built for evaluation.**

I. Introduction

THE high resolution, high efficiency positron emission mammography (PEM) system [1] and animal positron emission tomography (ANIPET) system [2] have been developed and constructed in Montreal Neurological Institute of McGill University. The detectors in PEM and ANIPET systems consist of bismuth germanate (BGO) crystal blocks optically coupled to Hamamatsu R3941-05 position sensitive photo-multipliers (PS-PMTs). The electronic circuits in the detectors include a Hamamatsu manufactured high voltage (HV) divider, crossed anode read-out resistor chain, positioning preamplifiers, and our developed fast timing amplifier circuit. The detector filed-of-view (FOV) is 56 × 64 mm. The timing resolution is 8.7 ns [3].

In order to improve the detector FOV and achieve better spatial resolution, we chose the latest small PS-PMT R7600-C12 [4] to build new high spatial resolution PEM and ANIPET detectors. The front-end electronic circuits for these new detectors have been designed. The circuits include modified HV divider, crossed anode read-out resistor chain with two schemes for evaluation, positioning preamplifier circuits with voltage feedback (VFB) amplifier, and timing preamplifier circuits with current feedback (CFB) amplifier.

A. Last Dynode output from HV divider

The purpose of modifying the HV divider is to supply an additional signal for event timing. Typically the timing trigger is acquired by discriminating the energy signal from anode output. Due to the multi-anode output structure in the PS-PMT, it will simplify the front-end electronics to take timing from one dynode output rather than from the summing of multi-anode signals.

The last dynode is chosen to take event timing because:

a. The dynode signal is synchronous with anode output so it can be chosen for anode timing measurement [5].
b. The signal taken from the last dynode has an amplitude comparable with that from the anode. It also has the highest signal-to-noise ratio compared with that from other dynodes.

B. The Anode Read-out Schemes

Many different schemes for anode readout circuits [6-10] are based on the fact that a PMT behaves as an almost perfect current generator - the anode current depends only on the incident flux and is completely independent of the load [5].

The common method of reading out anode signals from a PS-PMT is to combine all X or Y anode wires through a resistor divider chain. After the anode read-out circuit, there are only four positioning outputs (X–, X+, Y–, and Y+) regardless of the number of anode wires. Since the R3941 PS-PMT which we chose for PEM and ANIPET has eighteen X and sixteen Y anode wires, this method minimizes the number of processing signals effectively. The further compression approaches, like combining PMTs through common X and Y resistive dividers, have been investigated in the detector with multiple multi-channel PMT (MS-PMT) and PS-PMT applications [8-10].

In our new PEM and ANIPET scanner design, each new detector module includes sixteen R7600-C12 PS-PMTs. Even after combining all X and Y anode wires through the resistor divider chain, we still have to process 4 (X–, X+, Y–, and Y+) × 16 (PMTs) individual positioning signals in one detector module. So it is necessary to develop further compression methods to simplify electronics complexity.

We developed a method to simplify the positioning circuits by combining 4 PS-PMTs. With only four (X–, X+, Y–, and Y+) outputs, the new arrangements will reduce the number of processing signals by a factor of 4. Still with four fixed (X–,

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X+, Y−, and Y+) outputs, this method can be extended to achieve more compression by combining 9, or 16 PS-PMTs in the low count rate application.

C. Fast-slow Preamplifier Design

The fast-slow preamplifier design is generally applied in PET front-end electronics. The slow circuits are for position locating by integrating the anode outputs up to 800 ns in BGO scintillator applications [11]. The fast circuits are for timing processing to trigger the possible coincidence event.

In the nuclear detector field, positioning preamplifiers usually employ wideband JFET-input op amps because of their reduced input bias current. When precision is required, JFET op amps are generally inadequate due to their relatively high input offset voltage and drift [12]. Based on this consideration, our design uses high precision VFB amplifiers in the position charge sensitive preamplifier circuits.

In order to quickly respond the event timing, we chose the high bandwidth and ultra-fast setting time CFB amplifiers in our timing amplifier circuits. Compared with VFB amplifiers, CFB topology amplifiers have very low inverting input impedance and less effect on inverting input capacitance [13]. So they are especially suited to compensate the capacitance of the PMT. This specification meets our needs because we know the phase shift caused by the PMT capacitance is often a source of instability.

II. Materials and Methods

A. High Voltage Divider with Last Dynode Output

The Hamamatsu HV divider for R7600-C12 PS-PMT was modified in order to stretch out a signal from the last dynode for event timing. Fig. 1 shows the schematic.

The main problem of modification is how to obtain the signal from the last dynode without disturbing the anode signals. Compared with the manufactured HV divider circuit, three 0.01µF decoupling capacitors were changed from series decoupling to parallel. When 50Ω characteristic impedance coaxial cable is selected to transmit the dynode signal, a resistor of 200Ω to 300Ω (200Ω in Fig. 1) should be connected before dynode output. Because the last dynode still has about negative 30V voltage potential, a high voltage capacitor (0.02µ in Fig. 1) is used to AC couple the dynode output. The signal from the dynode has opposite polarity with that from the anode.

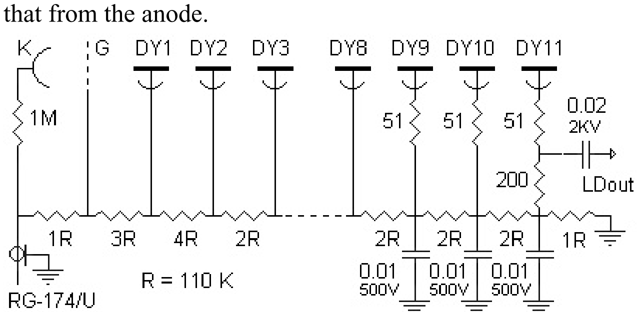

Fig. 1. This is the modified divider circuit. LDout is the last dynode output.

B. Position and Timing Preamplifier Circuits

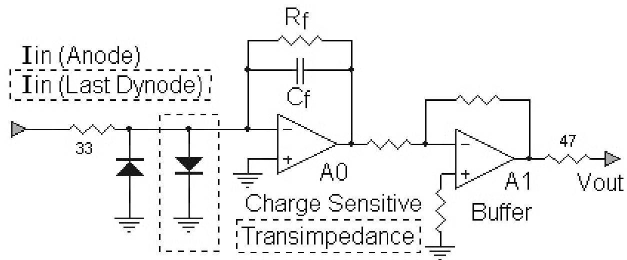

Fig. 2. This is schematic of positioning preamplifier with charge sensitive configuration, and timing amplifier with transimpedance configuration (illustrated in dotted frames).

Even though the schematics (Fig. 2) of the positioning integrator and timing amplifier circuits are quite similar, their concepts are different. Because the signal polarity from anode and last dynode is opposite, the layout of the protecting diodes (IN4145) in the two circuits are reversed. But the main differences are that the charge sensitive preamplifier with VFB is applied in positioning integrator circuit, and the current to voltage transimpedance preamplifier with CFB is chosen for our timing preamplifier circuit.

1) Position Integrating Pre-amplifier Circuits

The positioning preamplifier model is the classical second-order system. The output voltage magnitude (V_M) of the charge sensitive amplifier is:

$$Vm \approx Q/C_f \tag{1}$$

C_f is the feedback capacitor. Q is input charge with:

$$Q = \int_0^{t_w} i_t \cdot dt \tag{2}$$

where i_t is current output from the PMT anode, and t_w is the signal duration time. The feedback resistor R_f (~ 1M) discharges C_f (~ 1.2pF) in continues operation, and gives the DC negative feedback to stabilize DC working points.

Only VFB amplifiers are suitable for integrating purposes. The low bias current, high precision VFB amplifier CLC420, and the latest LT1880 [12] have been tested as integrator.

2) Timing Pre-amplifier Circuits

The CFB amplifier CLC450 was chosen to convert dynode current output to a fast response voltage. Compared with VFB amplifier, the CFB transimpedance amplifier gives a signal with a faster leading edge. So it is ideal for accurate timing. Another important feature of the CFB amplifier is that its inverting input impedance is very low. CFB amplifier has much less sensitivity to inverting input capacitance compared with the VFB amplifier. This is advantageous when using it in the inverting mode like a transimpedance I/V converter. In practice, a small value feedback capacitor C_f between 1.0 to 5.0pf is used to compensate for PS-PMT output capacitance.

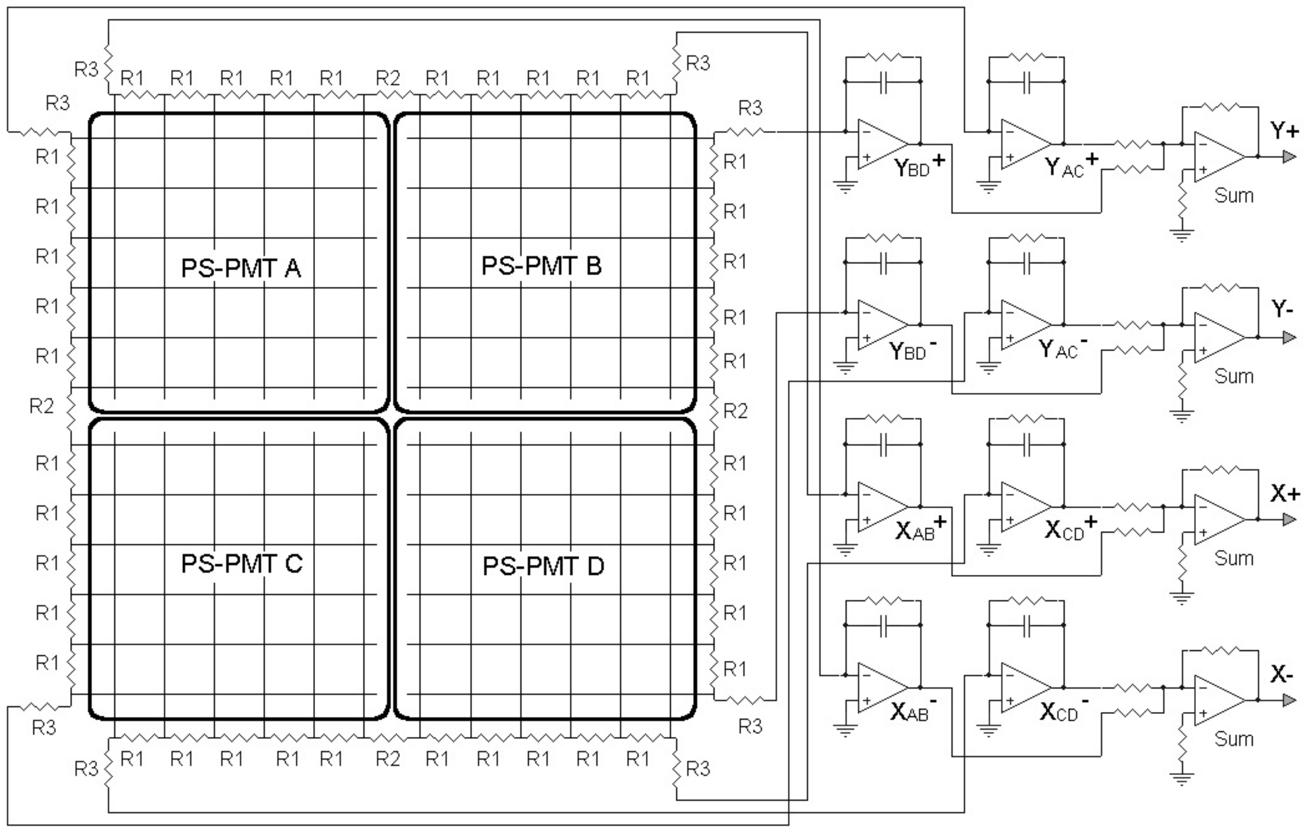

Fig. 3. Four PS-PMTs are combined together to build up as one block for further simplifying the positioning read-out circuits. All R1 resistors are 100Ω, R2 are 20Ω, and R3 are 70Ω. The charge sensitive preamplifiers are LT1880.

C. *Crossed Anode Read-out Configuration*

Pileup effect with a number of PS-PMTs in combination [10] is one issue we have considered in designing our detector structure. In our design, each detector array has been divided into four ideal modules. Each module consists four PS-PMT with separated electronics. Every module has its own timing signal, which can be independently coincident with one module in another detector array.

The detecting position accuracy is another issue we are concerned with. Because our BGO scintillation crystal has the complex dual-layer structure, the readout circuits should be capable of identifying all crystals.

Fig. 3 displays the 2×2 PMT scheme. PS-PMTs A and B (C and D) are combined through common X resistive dividers. PS-PMTs A and C (B and D) are combined through common Y resistive dividers. Eight charge sensitive preamplifiers integrate the resistive outputs. Still we have four X^+, X^-, Y^+, and Y^- positioning signals after four individual summing circuits.

These four PS-PMTs are built up as one detector module. The timing trigger is simply the sum of four last dynode outputs. After this arrangement, four PS-PMTs behave like a larger single PS-PMT with four (X^+, X^-, Y^+, and Y^-) positioning and one timing outputs. The positioning signals (X^+, X^-, Y^+, and Y^-) are digitized by the ADC module.

The event position is located by:

$$X = \frac{X^+ - X^-}{X^+ + X^-} \qquad Y = \frac{Y^+ - Y^-}{Y^+ + Y^-} \tag{3}$$

III. Results

A. *The Layout of Detector Units*

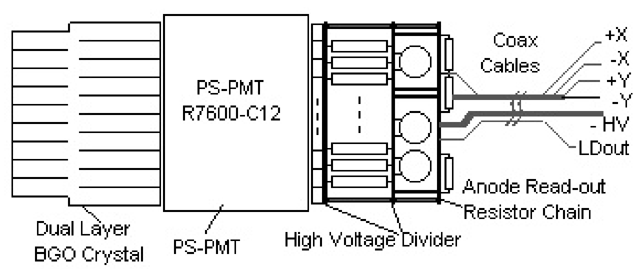

Fig. 4. This is the stack up layout of one detector unit. The unit includes a dual layer BGO crystal, PS-PMT R7600-C12, the HV divider and the anode read-out resistor chain circuits. Two circuit boards with connecting resistors and capacitors function as the high voltage divider. The layout is roughly to scale. The length of one unit is about 55 mm (before cables).

An individual detector unit is shown in Fig. 4, which includes a BGO dual-layer crystal, PS-PMT R7600-C12, the HV divider, and the anode read-out resistor chain circuits. Every four individual units are packed up into one detector module. Each module has its own positioning and timing electronic circuits with (X^+, X^-, Y^+, Y^-), and a timing trigger output. In total, four modules are combined to one detector array. Each module in one detector array can have coincidence with any module in another detector array. The coincidence events in different module pairs can be processed simultaneously. Fig. 5 illustrates the configuration of one detector array.

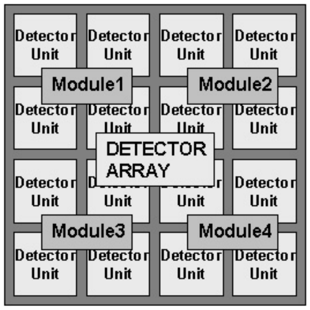

Fig. 5. This is configuration map of one detector array. Each array has four modules. Every module has four detector units. The unit is designed as "filed-replaceable unit".

B. The 2D Crystal Identification Image

The crystal identification image (Fig. 6) was by irradiating the crystal layer closest to the PMT with a collimated line source. An intensity profile along the white horizontal spline shows clear separation of the crystal elements.

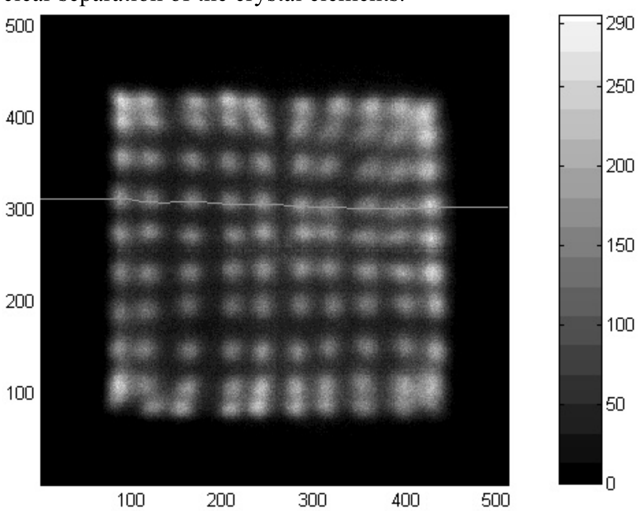

Fig. 6. This is BGO proximal layer crystal identification image. The 20×20×11 mm proximal layer crystal is cut to 10×10 crystal elements.

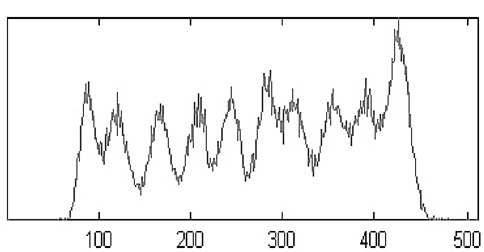

Fig. 7. This is the image profile of the white horizontal spline in Fig. 6.

IV. Discussion

Minimal detector dimensions are demanded, especially in the PEM scanners. So far we chose axial through-hole resistors and HV ceramic disc capacitors to build our HV divider circuits. The axial distances can be shortened by applying surface mount resistors and capacitors. The specific HV resistor network resistors manufactured with customer designed and ordered, which are commonly chosen in the commercial PET systems, can further shorten the divider length.

The method of combining four PS-PMTs has been proposed. With the tradeoff potential of more pileup effects, the circuits simplify the electronic processing signals. One consideration in our circuit is to modify the charge sensitive preamplifiers. The discharge resistor R_f (Fig. 4) generally is very big so the falling edge of A0 output is very slow with timing constant around 1μs. We will try other discharge schemes such as applying an analog switch [11], and using an additional non-inverting low-gain amplifier [14] in future experiments.

V. References

[1] C. J. Thompson, K. Murthy, Y. Picard, I. N. Weinberg, R. Mako, "Positron Emission Mammography (PEM): A Promising Technique for Detecting Breast Cancer," *IEEE Trans. Nucl. Sci.,* vol. 42, pp. 1012-1017, 1995.

[2] C. J. Thompson, P. Sciascia, K. Murthy, S. Kecani, L. Nikinnen, E. Campo, J-F. Corbett, Y. Bercier, M. Diksic, P. Cumming, "ANIPET: a Versatile PET Scanner for Imaging Small Animals," *IEEE Nucl. Sci. Symp. Conference Record,* vol. 2, pp. 1264 -1267, 1998.

[3] N. Zhang, C. J. Thompson, C. L. Thompson, K. Nguyen, "Improving the performance of small planar detectors for dedicated PET," *IEEE Nucl. Sci. Symp. Conference Record,* vol. 3, pp. 17_51-17_57, 2000.

[4] S. Nagai, M. Watanabe, H. Shimoi, H. Liu, Y. Yoshizawa, "A new compact position-sensitive PMT for scintillation detectors," *IEEE Trans. Nucl. Sci.,* vol. 46, pp. 354 -358, Jun 1999.

[5] Philips photonics, "Photomultiplier tubes: principles & applications," pp. 5.19, 5.21, 1994

[6] H. O. Anger, "Scintillation Camera," *Rev. Sci. Instr.* vol. 29, pp. 27-33, 1958.

[7] H. Kume, S. Muramatsu, M. Iida, "Position sensitive photomultiplier tubes for scintillation imaging," *IEEE Trans. Nucl. Sci.,* vol. 33, pp. 359-363, 1986.

[8] S. Siegel, R. W Silverman, Y. Shao, S. R. Cherry, "Simple charge division readouts for imaging scintillator arrays using a multi-channel PMT," *IEEE Trans. Nucl. Sci.,* vol. 43, pp. 1634-1641, Jun 1996

[9] N. K. Doshi, R. W. Silverman, Y. Shao, S. R. Cherry, "maxPET: a dedicated mammary and axillary region PET imaging system for breast cancer," *IEEE Trans. Nucl. Sci.,* vol. 48, pp. 811-815, June 2001.

[10] J. Seidel, J. J. Vaquero, F. Barbosa, I. J. Lee, C. Cuevas, M. V. Green, "Scintillator identification and performance characteristics of LSO and GSO PSPMT detector modules combined through common X and Y resistive dividers," *IEEE Trans. Nucl. Sci.,* vol. 47, pp. 1640 -1645, Aug. 2000.

[11] H. Li, W. H. Wong, N. Zhang, J. Wang, J. Uribe, H. Baghaei, S. Yokoyama, "Electronics for a prototype variable field of view PET camera using the PMT-quadrant-sharing detector array," *IEEE Trans. Nucl. Sci.,* vol. 46, pp. 546 -550, Jun 1999.

[12] G. Brisebois, "LT1880 SOT-23 superbeta op amp saves board space in precision applications, design note 266," Linear Technology Corp., 2001.

[13] W. Kester, "Section 1, High speed operational amplifiers," High speed design techniques, Analog Device Inc. pp. 18, 1996.

[14] A. Pullia, R. Bassini, C. Boiano, S. Brambilla, "A cold discharge mechanism for low-noise fast charge amplifiers," *IEEE Trans. Nucl. Sci.,* vol. 48, pp. 530-534, June 2001.