Digital Pulse Processor Using A Moving Average Technique

Valentin Jordanov and Glenn F. Knoll
The University of Michigan, Dept. of Nuclear Engineering, Ann Arbor, MI. 48109

Abstract

A digital pulse processor with improved differential linearity and reduced dead time has been designed. The circuit uses an 8-bit flash ADC running at 36 MHz and continually sampling the signal from the preamplifier or shaping amplifier. The digitized signal is then processed by a digital moving averager. A digital peak detector is used for measuring the amplitude of the shaped pulses. A novel, threshold-free circuit has been designed that combines both the moving average and peak detection functions. The circuit also provides a timing signal with an uncertainty of one sampling period. The number of the averaged samples (equivalent to the shaping time constant) is digitally controlled.

I. INTRODUCTION

Interest has recently grown in substituting purely digital methods for the analog techniques traditionally used in processing pulses from radiation detectors. Some of these are based on the analysis of digitized wave forms employing an off-line computer [1], and others use specialized on-line processors with relatively long processing times on the order of tenths of microseconds [2]. Other designs have been described [3,4] that are based on real-time processing on a faster time scale. However, these examples require the provision of a second, threshold sensitive, channel to generate the necessary control signal. As a result, these systems are more complex and subject to instabilities at low threshold levels [3]. This paper describes a simplified approach to real-time digital processing that is based on a combination of digital filtering and peak detection.

II. PULSE PROCESSING TECHNIQUE

One of the widely used technique for pulse filtering at high counting rates is the gated integrator (GI) [5]. An alternative approach to obtain the area under the detector pulse is to use a transversal filter with rectangular weighting function or moving integrator (MI) [6].

In a common spectroscopy system, where a threshold controlled ADC is employed to digitize the filtered signal, the gated integrator method offers higher throughput rate relative to the transversal filter approach. This comparison is illustrated in Fig. 1.

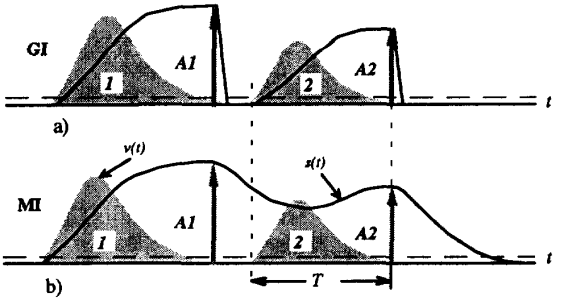

Fig. 1 Comparison between a) gated integrator and b) moving integrator.

Both MI and GI filters are characterized by an integration time T, equal to the width of the input pulse. Under these circumstances the MI shaped pulse is twice as long as the unshaped pulse. As a result the MI filtered pulses may overlap. However, the maximum amplitudes *A1* and *A2* (Fig. 1b) still will correctly represent the area under the pulses *1* and *2*. If the shaped signal shown on Fig. 1b) is processed by a traditional, threshold based, ADC the second peak (*A2*) will be lost, although it is a correct measure of the area of pulse *2*. To eliminate this shortcoming we propose to use a threshold-free measuring system based on peak detection and utilizing a moving average technique.

A. Pulse Integration

The moving integrator output $s(t)$ can be expressed as a convolution of rectangular function and the input signal $v(t)$ [5]. The convolution integral has the form

$$s(t)=\int_{t-T}^{t} v(\tau)\cdot d\tau \qquad (1)$$

where T is the width of the rectangular function. Equation (1) can be rewritten as a difference of two integrals

$$s(t)=\int_{0}^{t} v(\tau)\cdot d\tau-\int_{0}^{t-T} v(\tau)\cdot d\tau\ . \qquad (2)$$

When the following condition is met

$$v(t)=0 \text{ for } -T\leq t<0 \qquad (3)$$

then equation (2) can be expressed as

0-7803-0883-2/93/$3.00 ©1993 IEEE

$$s(t)=\int_0^t [v(\tau)-v(\tau-T)]\cdot d\tau \qquad (4)$$

The function *s(t)*, described by equation (4) has an extremum if $ds(t)/dt=0$ or $v(t)-v(t-T)=0$. Therefore, *s(t)* reaches its maximum value when the signal *v(t)-v(t-T)* crosses zero and changes its sign from positive to negative.

B. Moving Average

In the discrete-time case, equation (4) can be approximated by a sum of equally spaced samples of the signal *v(t)*

$$s[n]=\sum_{i=0}^{n}\{v[i]-v[i-k]\}, \qquad (5)$$

where the constant k is the number of the samples corresponding to the integration time window.

The sum $s[n]$ reaches its maximum value at n_p if

$$\left\{\begin{array}{c} s[n_p]-s[n_p-k]\geq 0 \\ s[n_p+1]-s[n_p+1-k]<0 \end{array}\right\} \qquad (6)$$

Hence, in order to apply the MI technique and to detect the peaks in the shaped signal, a difference between prompt and delayed input signal should be carried out. This difference is continually added to the content of a digital accumulator. In our particular case the accumulator sum is normalized to the range of the ADC.

III. REALIZATION OF THE PULSE PROCESSOR

A block diagram of the circuit used to investigate our approach is shown in Fig. 2. The circuit is initialized by activating the *RESET* signal. Upon reset, the accumulator, input register and data pipeline are cleared, thus the necessary condition (3) is fulfilled.

The voltage pulse from the preamplifier or fast shaping amplifier is first digitized in a 36 MHz flash ADC. The output of the ADC is connected to the data input of an edge triggered register. The code from the input register is applied both to one input of a digital subtraction unit and to a digital pipeline with programmable depth [7]. The output of the pipeline is then applied to the second input of the subtraction unit. Through this operation, the delayed signal is subtracted from the prompt ADC code. The result (including algebraic sign) is added to the content of a digital accumulator. The output of the accumulator represents the equivalent of the filtered signal. The accumulator content is then scaled down to the range of the ADC and is applied to the output FIFO register.

The peaks in the filtered signal are detected by the LOW to HIGH transition of the *PEAK* signal which follows the changes in the sign signal SIGN. In order to avoid false peak detection, measures have been taken to prevent *PEAK* signal change when the difference *A-B* is equal to zero by holding its value to that in place in the previous iteration (clock cycle).

When the signal PEAK changes from LOW to HIGH, the content of the accumulator has reached a maximum. This transition of the signal *PEAK* is used to generate (Fig. 2, D-trigger U1, NAND gate U3) a one cycle wide pulse *WRITE* which enables a write operation into the output FIFO register, thus storing the peak value of the pulse. In order to improve the noise immunity, the LOW level at the inverting output of U1 could be extended with a time interval slightly shorter than the integration time interval *T*. If there is an overflow in the time interval between two adjacent peak detections, the second pulse will be recorded as an overflow event. The FIFO register is read by an external MCA circuit.

If the processing time of this circuit is sufficiently short then all of the detected events will be stored; otherwise some events my be lost. In the second case a digital threshold circuit might be used, following the FIFO register.

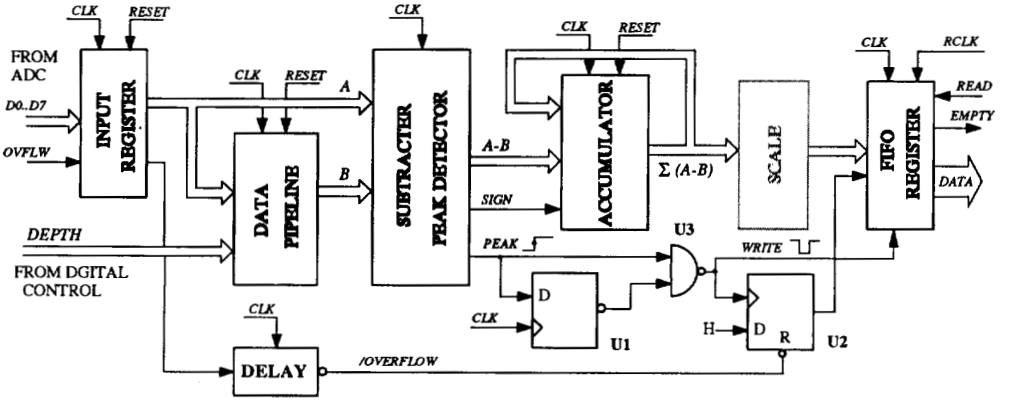

Fig 2 Block diagram of the digital pulse processor

In addition, a timing signal can be derived from the *PEAK* signal that will be accurate to within one clock cycle.

The system is operated under full digital control, including the choice of data pipeline depth. This value can be selected to be any binary number from 1 to 254 samples. In the limit of small values, the circuit functions as a simple peak detector.

IV. Preliminary Test Results

A prototype of the processor was built using high speed PLD's and fast TTL integrated circuits. The design allows the circuit to operate at clock frequencies up to 65MHz. The prototype operates with 8 bit input data; however the data width is expandable to 12 bits without reducing the sampling frequency.

One of the benefits of using digital integration technique is the improved differential nonlinearity (DNL) [3]. DNL was estimated using a custom built tail pulse generator producing pulses with uniform distributed amplitudes. Fig. 3 shows the results of a differential nonlinearity test. Case a) represents the simple peak detector DNL which is equal to the DNL of the ADC. It is seen that the DNL improves when the averaging technique is used (Fig. 3b). The integral

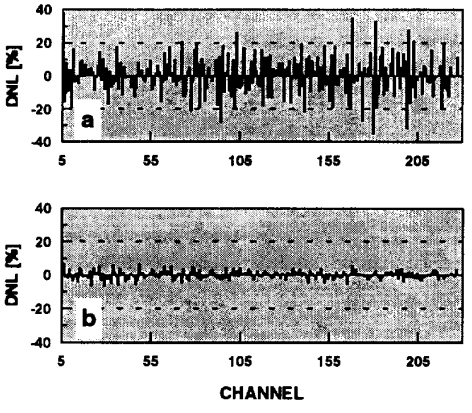

Fig. 3 Differential nonlinearity: a) DNL=35% ±1.5%, k=1; b) DNL=6% ±1.5%, k=36.

nonlinearity of the processor was also measured using calibrated tail pulse generator and was found to be less than 0.5%.

The major limitations of the processor are the ADC resolution and the finite sampling frequency. The device was tested using a Cs-137 source and NaI(Tl) scintillation detector. An energy resolution of 6.4% at 662 keV was obtained using a conventional quasi-gaussian filter with 1.5μs shaping time constant. The pulses from the detector have 90 ns rise time (10%-90%). The integration time was $t_c \cdot k=1$ μs. The results for the energy resolution that was observed using the digital processor as a function of the clock frequency are presented in Fig. 4.

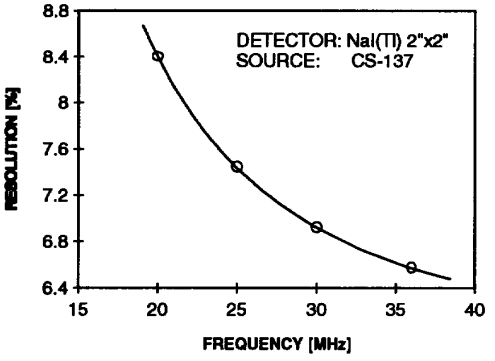

Fig. 4 Energy resolution vs. sampling frequency.

The energy resolution of the pulse processor improves with increasing sampling frequency because the area under the pulse is estimated using more samples. There is another source of error due to the fact that the processor clock and the pulse arrival time are not synchronized. This error also decreases with increasing sampling frequency.

V. Conclusion

A real time digital pulse processor using a moving average technique has been designed. A threshold-free approach has been used for decreasing pileup losses. The processor was shown to be effective in reducing differential nonlinearity. The resolution of the processor is limited by the finite ADC resolution and the finite sampling frequency. Increasing the sampling frequency should improve the resolution in pulse height analysis and the timing precision.

V. References

[1] V. Drndarevich, P. Pyge and T. Gozani,, "Digital signal processing for high rate gamma-ray spectroscopy", *Nucl. Instr. and Meth.*, vol. A277, pp. 532-536, 1989.

[2] T. Lakatos, "Adaptive digital signal processing for x-ray spectrometry", *Nucl. Instr. and Meth.*, vol. B47, pp. 307-310, 1990.

[3] F. Hilsenrath, H. D. Voss, and J. C. Bakke, "A single chip pulse processor for nuclear spectroscopy", *IEEE Trans. Nucl. Sci.*, vol. NS-32, pp.145-149, February 1985.

[4] J. S. Karp et al., "Event localization in a continious scintillation detector using digital processing" *IEEE Trans. Nucl. Sci.*, vol. NS-33, pp.550-555, February 1986.

[5] V. Radeka, "Trapezoidal filtering of signals from large germanium detectors at high rates", *Nucl. Instr. and Meth.* vol. 99, pp. 525-539, 1972.

[6] G. L. Miller and D. A. H. Robinson, "Transversal filters for pulse spectroscopy", *IEEE Trans. Nucl. Sci.*, vol. NS-22, pp. 2022-2032, October 1975.

[7] V. Jordanov, "Data Pipeline with Programmable Depth", *Electr. Design News*, (in press)