A Data Acquisition System for a Ring Compton-Scatter Camera

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Abstract

A data acquisition system for a Ring Compton scatter Camera (RCC) has been developed. The RCC is composed of two detector arrays. A personal computer is used for storing the detector energy data and controlling the Compton camera. The camera output interface uses a pipelined hardware architecture to reduce the counting losses due to the finite data transfer time, and to provide variable length data records to the computer. Data transfers are controlled by either hardware or software generated interrupts. The acquisition modes include: the collection of coincident spectra, delayed coincident counting curves, and pulse height spectra from the individual detectors. Diagnostic procedures have also been developed. The software supports all of the hardware functions, and provides routines for preprocessing and displaying the acquired data.

I. INTRODUCTION

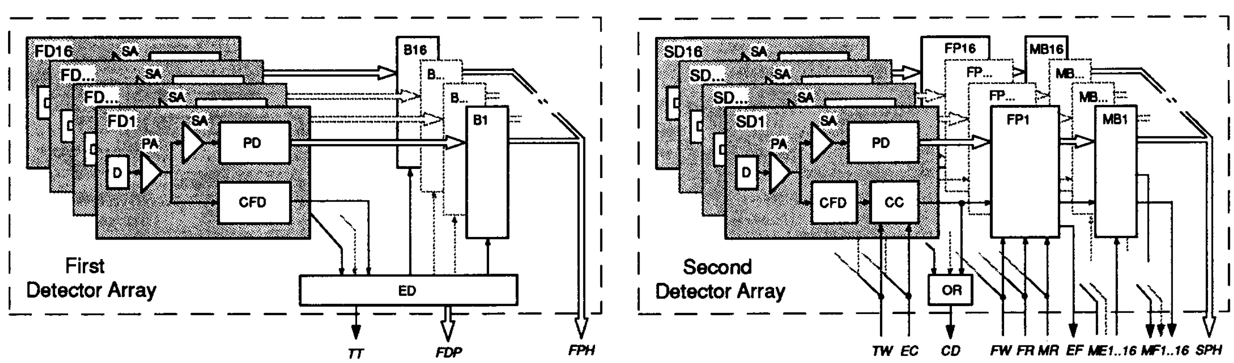
The RCC is a gamma-ray imaging system using two coordinated arrays of radiation detectors [1,2]. A gamma ray incident on the camera can be imaged when it Compton scatters from an HPGe element in the first array and is then absorbed in an NaI(Tl) element of the second array. To image incident gamma rays from these scattering events, the position of the elements in which the gamma ray interacted, and the energy deposited in both elements must be recorded. In order to distinguish between valid imaging events and random background events, two criteria are applied. First, only coincident interactions in first and second detector are recorded. Secondly, the sum of the energies deposited in the first and the second detector needs to be equal to the energy of the interacting gamma quantum. While the event selection based on the first criterion is done by the hardware, the energy criterion requires either a complex hardware solution [3], with limited performance, or software implementation using a computer. The computer solution becomes essential when multi-energy gamma-ray fields are imaged.

A hardware system to process the RCC events has been developed and interfaced to a personal computer where the data are preprocessed and stored for off line image reconstruction.

II. SYSTEM HARDWARE

Fig. 1a shows a principle block diagram of the first detector array. The signals from sixteen HPGe elements are processed by front-end electronics units (**FD1..16**). Each of those units consists of a preamplifier (**PA**), a shaping amplifier (**SA**), a peak digitizer (**PD**) and a constant fraction discriminator (**CFD**). **CFD** generates a timing signal while **PD** provides 8-bit pulse height data. The outputs of **CFD** are applied to an encoder (**ED**) which generates a timing signal, associated with the first element that fires. **ED** also delivers a digital code (*FDP*) corresponding to the array position of the element triggered the timing signal. The pulse height data of the active detector element are applied to an 8-bit data bus (*FPH*) through a buffer (**B1..16**). An internal one-shot trigger is used to hold the pulse height data for a fixed time, which is set slightly longer than the time required for the data from the second detector to be properly recorded.

The block diagram of the second detector array is presented in Fig. 1b. This array consist of sixteen individual NaI(Tl) detectors which are connected to front-end electronics, similar to that of the first detector array.



a) b)

Fig. 1 A block diagram of the first (a) and the second (b) detector arrays.

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However, an additional coincidence circuit (CC) is incorporated. A timing reference signal (*TW*) is applied to the CC. When a coincidence is indicated the output of CC is activated and is held at this state until reset signal *EC* is applied. The pulse height code from the peak digitizer is passed through a FIFO based pipeline (**FP1..16**), and then applied to a mailbox circuit (**MB1..16**). The data are written and read in **FP** by activating signals *FW* and *FR* respectively. *MR* is the master reset signal and *EF* is an empty indication signal. The **OR** circuit generates a trigger signal (*CD*) with the first NaI(Tl) detector element that fires in coincidence with the HPGe detector. **MB** provides a signal *MF* indicating that the corresponding mailbox contains pulse height data of a coincidence event. The mailboxes are three-state registers (74F755) whose outputs are enabled by activating one of *ME1..16* lines. When a given mailbox is read (outputs are enabled) the corresponding mailbox flag *MF* is cleared [4]. Thus, a simple circuit for polling only the active mailboxes can be designed. In our approach the mailbox flags are applied to a priority encoder. The binary encoded signal is then decoded and stored in an edge triggered register. As a result, for each coincident event, only the active mailboxes are read.

A simplified block diagram of the acquisition system is shown in Fig. 2. The data from the first detector array passes through a pipeline (**FPL**) similar to that of the second detector array. The timing signal *TT* from the first detector array is delayed in a digitally controlled delay line (**DL**), and a coincidence timing window is generated by a pulse generator (**WG**). When one or more second array elements are in coincidence with the first array, *CD* is activated, storing the current pulse height data in the pipelines. After a short delay (slightly longer than the timing window), the CC in the second array are reset and the system is ready to record the next event. Thus, the resolving time of the system for two consecutive events is limited only by the finite shaping time of the front-end electronics.

Data from the detector pipelines are transferred to a second output pipeline (**OP**). This process is controlled by an interface control unit. Fig. 3 shows a generalized flowchart of the operational principle of this control unit. If the data is present in the detector pipelines (*EF* not active), a read operation is performed, and all the data corresponding to one coincident event are transferred into the mailboxes *MB0..16*. Further, the detector position and pulse height code from the first detector array are stored in two bytes of the **OP**. Next

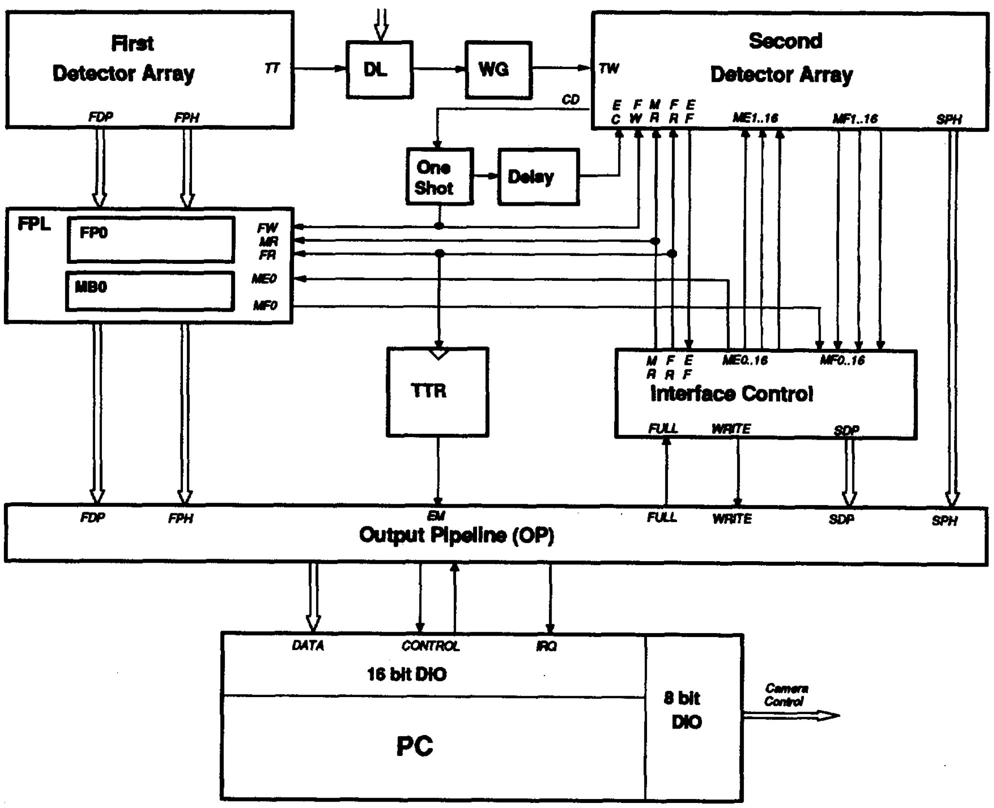

Fig. 2 A block diagram of the acquisition system for the RCC.

the information from the second array is read. In order to reduce the data transfer time only the active mailboxes are read. The interface control unit also generates a position code, *SDP*, corresponding to the currently read mailbox.

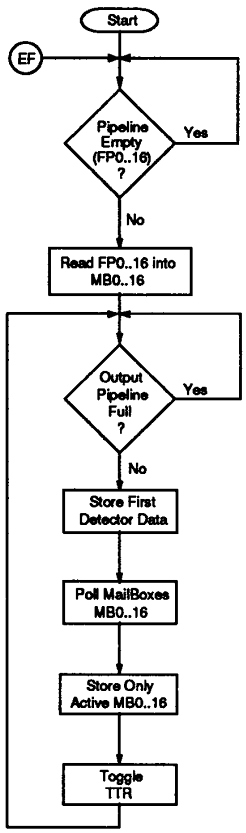

Fig. 3 Interface control flowchart.

Two data bytes from the second array are stored in queue fashion following the data from the first array. Because of the chance coincidence rate and multiple scattering interactions, the number of the detectors from the second array, which are in coincidence, may vary from one to sixteen for each recorded event. In order to distinguish between different events a T-trigger (**TTR**) is toggled after each event record is completed. The **TTR** output is stored as the most significant bit in the detector position byte of the **OP**. The software identifies a new event record when that bit changes. The half-full flag of the **OP** is used for generating an interrupt signal, initializing a software data reading routine. The **OP**, when not empty, could be also read by a software driven interrupt routine. The coincident data is transferred from the RCC hardware to the computer through a Computer Boards CIO-PDMA16 digital IO interface card [5].

The computer also provides control signals to the RCC. These control signals are supplied to the RCC through the parallel printer port of the computer, and are used to enable the individual elements in the first and second detector arrays. The computer also controls the coincident delay time between the two detector arrays.

III. Acquisition and Control Software

The acquisition software is written in C++ and is executed on a 486-33MHz microcomputer. The primary task for the computer is to collect and store coincident event data. Each event consists of two or more (up to 16) data words. The first word contains the detector number and energy from the first, HPGe array, while the rest of the words contain the same information for the coincident elements of the NaI(Tl) array. Once the binary data have been transferred to the computer, the HPGe and NaI(Tl) pulse heights are converted into energies using pre-measured calibration curves and added together to find the summed energy of the incident gamma ray. Software utilities have been written to histogram and display the summed energy data. The summed energy spectrum is also used to select specific gamma-ray full energy peaks for image reconstruction. This function is critical for imaging multi-energy gamma-ray fields.

The pipelined organization of the acquisition hardware frees the computer from having to continuously monitor the DIO card for new data. Instead, the acquisition can be performed using an interrupt service routine. The use of interrupt handlers to acquire the coincident and calibration data from the RCC serves two purposes. First, it frees the computer to perform other tasks and run other applications during acquisition which may last several hours. This also allows the control routine to monitor the performance of the individual detectors and the camera as a whole To monitor the individual detector elements, total counts in each element are displayed using a color map. From this display, malfunctioning elements can be easily identified. The total system counts and the summed energy histograms can also be monitored to give indications of the overall system performance.

The interrupt service routine functions by transferring a block of coincident data from the RCC output buffer into the computer memory when an interrupt is received. In the RCC system, the interrupt signal is created in one of two ways. First, the signal from the RCC hardware can be used to interrupt the computer and have it initiate a data transfer. This RCC interrupt signal is produced by the systems hardware when the buffer becomes half full. In this approach, the interrupt handler simply reads in half of the buffer and then returns, creating a very fast and efficient implementation. A second method for generating the interrupt signal is to have it created internally by the computer's timer circuitry. In this approach, the computer polls the buffer at regular time intervals, transferring any new data from the output buffer to computer memory. This routine is not as efficient as the first because each time it polls the buffer, it must determine whether the buffer is empty. The internal timer implementation also suffers when the event rate is not significantly greater than the timer interrupt rate. In this case, the interrupt handler is entered more times than with an external interrupt for the same number of valid events. This limitation can be overcome by monitoring the number of events received during several consequent timer interrupts and then adaptively adjusting the interrupt interval. Using this adaptive implementation, the timer routine efficiency is again only limited by having to check whether the buffer is empty.

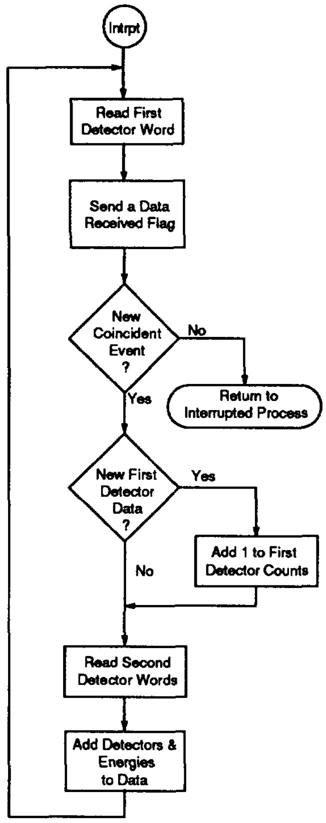

Fig. 4 Interrupt routine flowchart.

The flowchart for the timer interrupt routine is depicted in Fig. 4. Once an interrupt is received, the first data word is read from the output buffer and the received flag is set. The first word holds the HPGe detector number and energy. The data is checked to determine if this is a new event, if it is, the words holding the NaI(Tl) data are read, otherwise the routine exits. Once both words are read, the data is transferred to memory, and the procedure is repeated. The external interrupt solution is similar, except that the first word no longer needs to be tested, and the loop is continuously executed until half of the buffer is read.

Both of the interrupt handling routines have been implemented with this system. The hardware interrupt handler was included in a DOS version of the RCC control program. In this routine, the maximum collection rate achieved was 7,800 events per second. The timer interrupt handler is currently used with the WINDOWS version of the RCC control program and the maximum collection rate was found to be 5,500 events per second. It is easily seen that the acquisition rate improves using the external interrupt routine, and we expect to use this as the primary acquisition routine in the final version of the code. The acquisition rate can also be increased using DMA transfers. This has not yet been investigated but is under consideration for future versions of the RCC acquisition system.

IV. APPLICATION

As suggested in the introduction, an important application of the RCC is imaging of multi-energy gamma-ray fields. Fig. 5a shows an autoradiograph of a radioactive phantom, taken by exposing photographic film with the radiation. The phantom consists of a U-shaped source which emits 1.116 MeV photons and an M-shaped source which emits 0.511 MeV photons. The two sources in the phantom were imaged simultaneously with the RCC, and reconstructed images of the 1.116 MeV photons and the 0.511 MeV photons are shown in Figs. 5b and 5c, respectively. Separation of photons from the two sources is achieved by summing the energy deposited in both detectors of the camera by each coincident event, and selecting events that fall within energy windows set about the energies of interest.

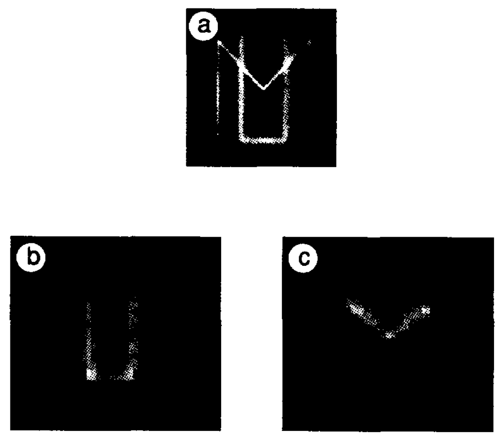

Fig. 5. Example images of a multi-energy gamma-ray phantom measured with the RCC. (a) Autoradiograph of phantom with a U-shaped source that emits 1.116 MeV photons and an M-shaped source that emits 0.511 MeV photons. (b) Reconstructed image of 1.116 MeV photons. (c) Reconstructed image of 0.511 MeV photons,

V. Conclusion

A data acquisition system for a RCC has been developed. A pipelined architecture is used to reduce counting losses. A mailbox based interface allows to store variable length data records, minimizing the data transfer time and required computer memory space. All of the acquisition system functions are supported by the software. In addition many of the camera operating modes are remotely controlled and the system performance can be monitored with the software. Efficient interrupt routines have been developed to achieve acceptable throughput rates.

VI. Acknowledgments

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VII. References

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