AGET, a Front End ASIC for Active Time Projection Chamber

Data Sheet

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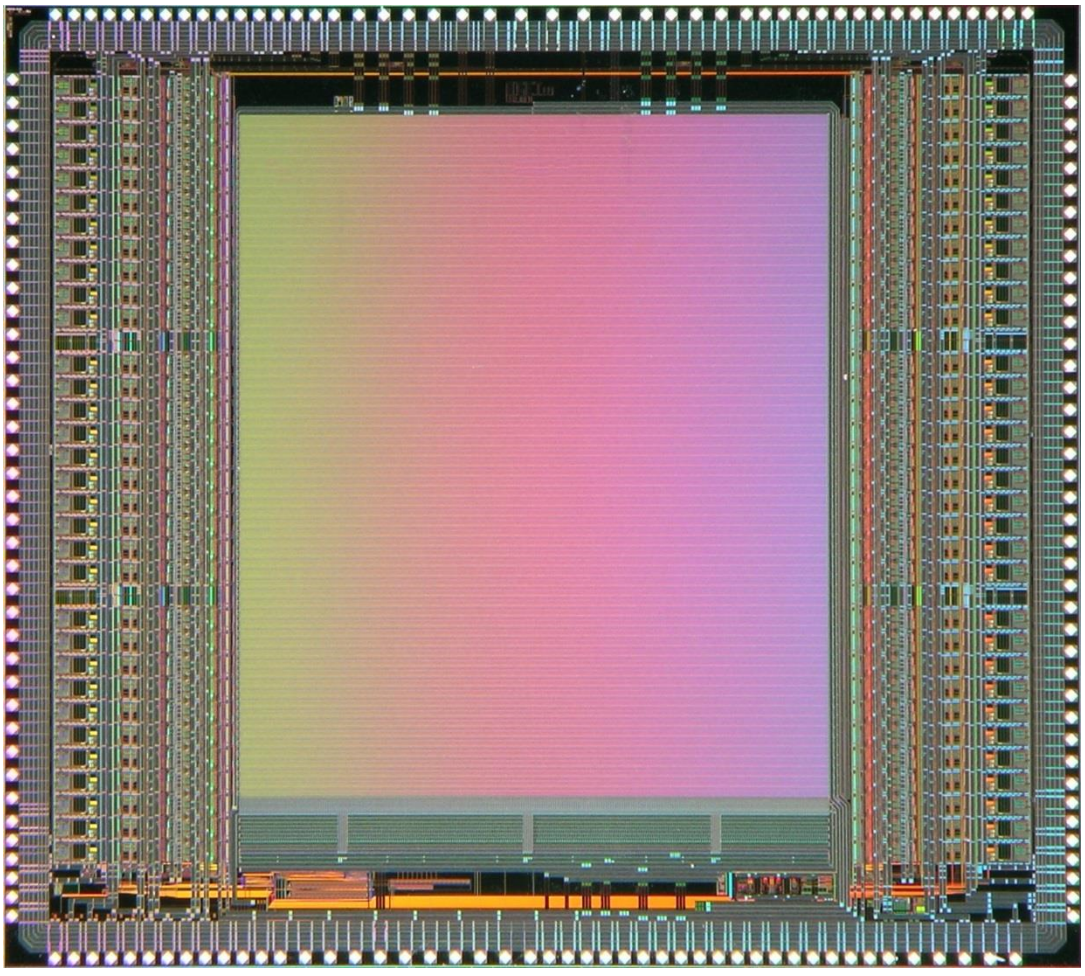


Revision history

Date	Revision	Changes
24-Sept-12	1.0	Creation of the document
10-Jan-13	2.0	Corrections (Thanks to Abu-Nimeh Faisal MSU)
25-Nov-15	3.0	Additional documents about : • AGET input impedance & external coupling • AGET in positive polarity mode • Note on the Multiplicity signal

A number of modifications has been made on this production version compared to the previous prototype version [Annexe 1]. The prototype version has been tested successfully and the main results are reported in a paper of IEEE conference [ref.1].

At the end of this document are reported three additional documents.

The first concerns the description of the input channel and the effect of DC input current. It gives also some recommendations in the case where external coupling is used.

The second gives recommendation in the case where the positive polarity mode is used and the last document describes how to tune the amplitude of multiplicity unity signal.

Contents

1. Introduction

This document gives a full description of the AGET (**A**SIC for **G**eneral **E**lectronics for **T**PC) chip. It must perform the amplification, the detection and the analog storage of the shaped detector signal before its digitization by an external ADC. The architecture is based on the one of the AFTER chip [ref.2] with significant new features and modifications to match different detectors (gain and drift time), detect the signal (trigger & hit channel address), support the different kinds of particles (charge) and also the different kind of nuclear reactions (2p radioactivity).

Four of these devices (**Fig. 1**) are soldered on the AsAd (**A**SIC **S**upport & **A**nalog-**D**igital conversion) card with four 12-bit ADC (one per AGET). The digital outputs of the 4 ADCs are transmitted by 8 differential lines with a maximum speed of 1.2 Gbit/s to the CoBo board.

The CoBo (**Co**ncentration **Bo**ard) board is responsible for applying a time stamp, zero suppression and compression algorithms to the data. It will also serve as a communication intermediary between the AsAd and the outside world. The slow control signals and commands to the AsAd will be transmitted via the CoBo (four AsAd per CoBo).

The Mutant (**Mu**ltiplicity **T**rigger **An**d **T**ime) card manages the multiplicity, the conditions for the trigger, and the distribution of the clock on the whole system. The global data is transmitting through network switch to computer farm.

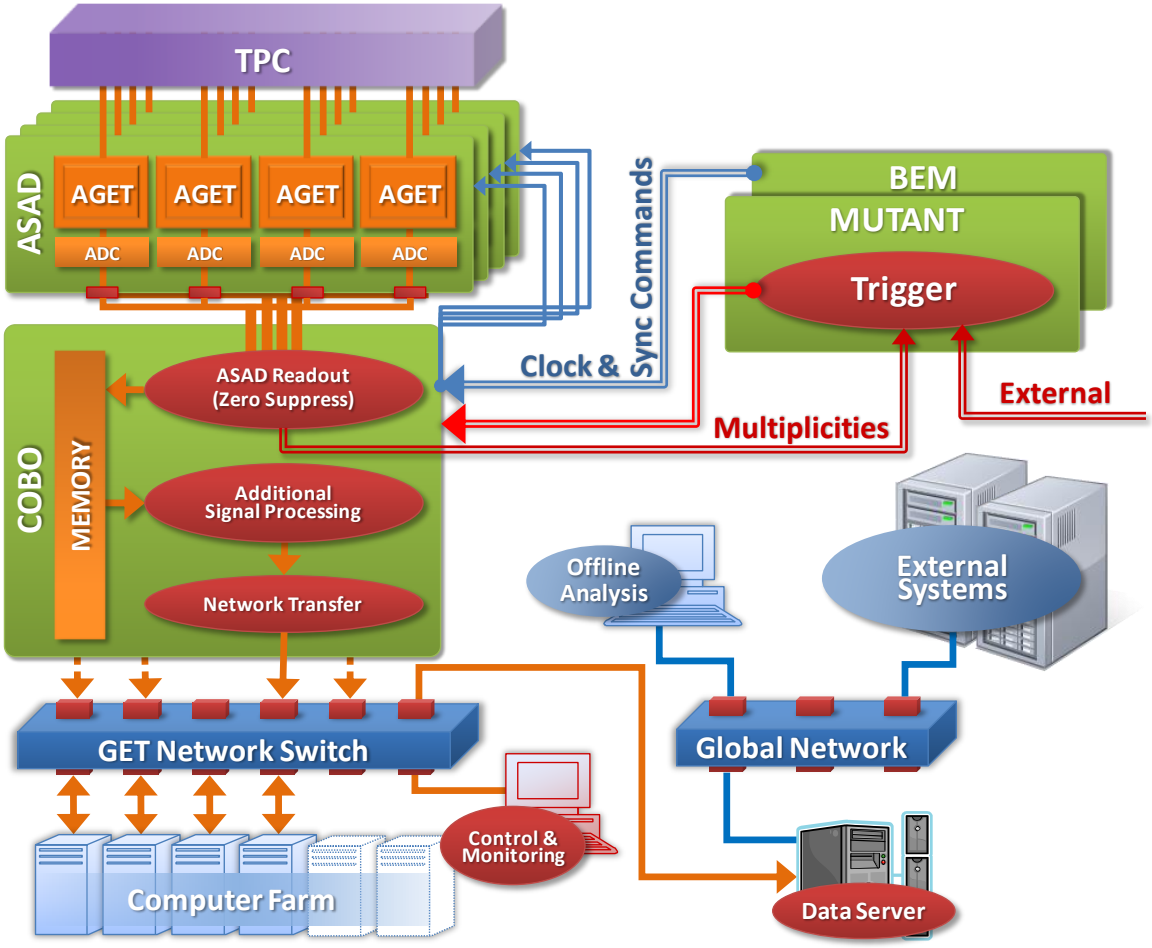


Fig. 1: Global view of the GET electronic.

1.1 AGET general description

The ***AGET*** chip has **64** channels (**Fig. 2**), each one is connected to a detector pad. A channel integrates mainly: a charge sensitive preamplifier, an analogue filter (shaper), a discriminator for trigger building and a 512-sample analog memory.

The charge sensitive preamplifier (CSA) has variable gain to support the dynamic range of 120 fC to 10 pC. This gain is adjusted per channel, by selecting one of the four CSA feedback capacitors (ASIC Slow Control).

The analog filter is formed by Pole Zero Cancellation stage followed by a 2-complex pole Sallen-Key low pass filter. The peaking time of the global filter is selectable among several values (16 values) in the range of 50 ns to 1 µs. The filtered signal is sent to the analog memory and discriminator inputs.

The memory is based on a **S**witched **C**apacitor **A**rray structure (**SCA**) and used as a 512 cell-depth circular buffer, in which the analog signal coming out from the shaper is continuously sampled and stored. The sampling frequency can be set from 1 MHz to 100 MHz to match with the various drift velocities of the chambers. The sampler is stopped on an external trigger decision. In the read out phase, the analogue data will be, in time domain, multiplexed toward a single output and sent to the external 12-bit ADC at the readout frequency range of 25 MHz. There are three different modes for the read out of the SCA channels: all the channels, hit channels or specific channels. In conjunction with this channel readout mode, it will be possible to read the SCA according to a predefined number of analog cells (1 to 512).

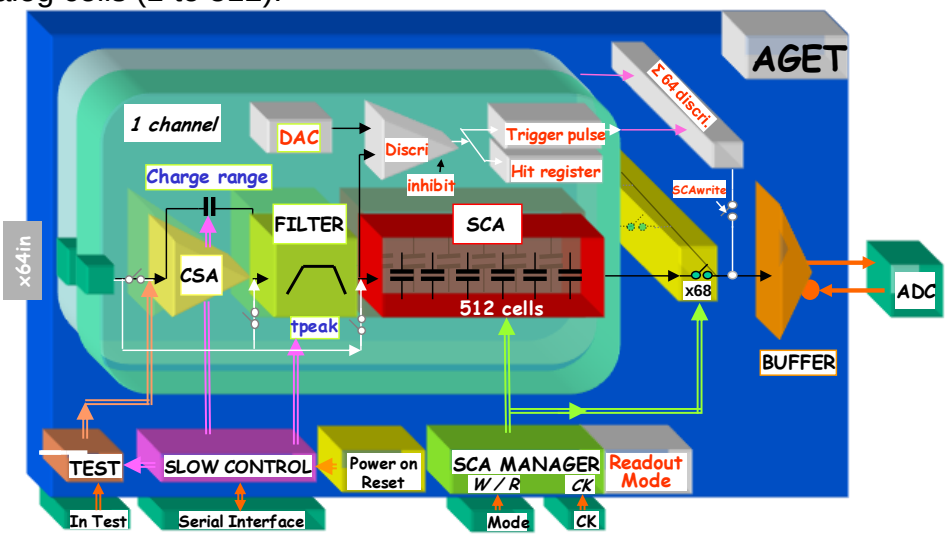


Fig. 2: **Block diagram of the AGET chip.**

The filtered signal, through a differential gain stage, is compared at the discriminator block to a programmable threshold value (7-bit DAC + 1 polarity bit). This value is set by 2 internal programmable DACs. The 4 bits of the first one, common to the 64 channels, define the 3 MSB bits of the threshold value and the polarity of the input signal. The second DAC is attached to the channel and defines the 4 LSB bits of the threshold value. If the signal crosses the threshold, the discriminator output signal sets the hit channel register to an active level and forms with the 63 others discriminator signals a multiplicity signal (analogical sum) with a defined value or not (ToT). During the SCA writing phase, this signal is continuously digitizing by the same external 12-bit ADC and analyzed on line to build a trigger signal.

The output signal of the discriminator sets a temporary register during a programmable time defined by the address column pointer of the SCA (“0”, “128”, “256” or “384”). If a second event arrives when the temporary register is busy, the memory time

is increased again. On the falling edge of the SCA write signal, this register output is memorized in the hit-channel register. This hit-channel register could be read or modified after the SCA writing phase by using the ASIC slow control link (with a specific protocol).

To process two consecutive events (implantation & decay event) in a time window less than 1 or 2 ms, it will be possible by slow control to split the SCA memory in two separate blocks. Each block will be dedicated to sample and store its event until the readout phase where the two memories will be read.

A SPI compatible serial link is used to configure the chip parameters (e.g. gain, peaking time, test, readout mode). Two chip inputs permit to calibrate or to test the channels. A "spy" mode is available to control some internal test points (CSA & PZC outputs; SCA & discriminator inputs) of the first analogue channel or of the sum of the 64 individual "trigger" signals.

To cope with the various detector configurations, this ASIC can operate with both signal polarities according to the values of the DC voltages inside the chip. It is also possible to bypass the internal CSA of the channels to access directly to the filter or SCA inputs.

1.2 AGET mode of operation

The AGET circuit is controlled by CoBo board through the AsAd card. As shown in **Fig. 3**, a limited number of signals are necessary to manage it: 2 for the electric test & calibration, 4 for slow & hit channel control, 4 for the SCA write & readout and 1 for the trigger & SCA data output.

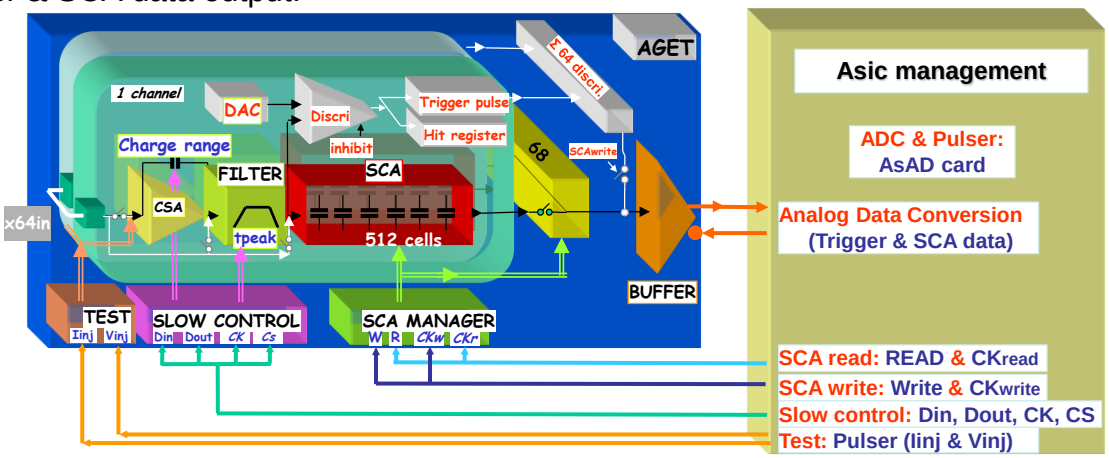


Fig. 3: Schematic of the AGET control.

The different functionality phases (**Fig. 4**) are:

1. The sampling in the SCA & signal detection are enabled,
2. If a signal appears at the input of a channel:
3. The input signal is filtered, amplified and sampled in the channel SCA,

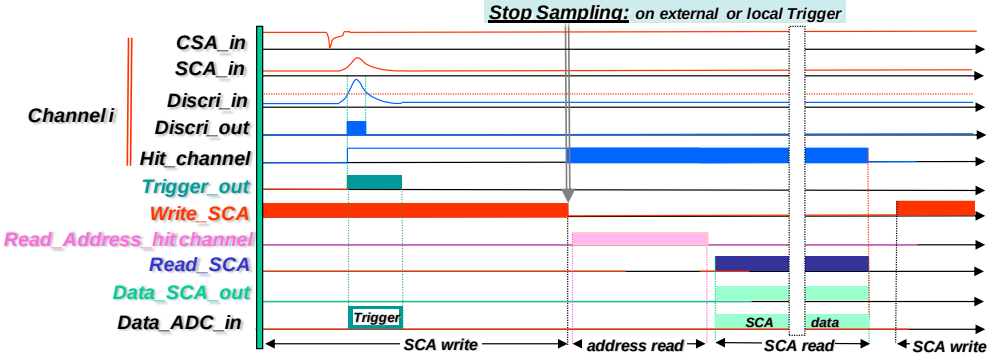


Fig. 4: Chronogram of the AGET operating modes.

4. If the charge is higher than a minimum value, the channel gives a unity trigger signal which is digitized by the external ADC,
5. If this signal is considered as a good event or on external trigger, the SCA sampling is stopped, and the trigger signal memorized in the hit channel register,
6. A readout of the hit channel registers and/or a write of the selected channel address can be performed,
7. The readout of the SCA analog data is done, and all the cycle can restart again.

1.3 AGET requirements

The main specifications and requirements for the AGET chip have been defined in January 2009 [ref.3] and are summarized in the table 1.

Parameter	Value
Polarity of detector signal	Negative or Positive
Number of channels	72
External Preamplifier	Yes; access to the filter or SCA input
Charge measurement	
Input dynamic range	120 fC; 1 pC; 10 pC
Gain	Adjustable/(channel)
Output dynamic range	2V p-p
I.N.L	< 2%
Resolution	< 850 e- (Charge range: 120fC; Peaking Time: 200ns; Cinchannel. < 30pF)
Sampling	
Peaking time value	50 ns to 1 µs (16 values)
Number of SCA Time bins	511
Sampling Frequency	1 MHz to 100 MHz
Time resolution	
Jitter	60 ps rms
Skew	< 700 ps rms
Trigger	
Discriminator solution	L.E.D
Trigger Output/Multiplicity	OR of the 72 hit channel registers; Width = 2xTSCAckread
Dynamic range	5% of input charge range
I.N.L	< 5%
Threshold value	4-bit DAC/channel + (3-bit + polarity bit) common DAC
Minimum threshold value	≥ noise
Readout	
Readout frequency	20 MHz to 25 MHz
Channel Readout mode	Hit channel; specific channels; all channels
SCA Readout mode	511 cells; 256 cells; 128 cells
Test	
calibration	1 channel / 72; external test capacitor
test	1 channel / 72; internal test capacitor (1/charge range)
functional	1, few or 76 channels; internal test capacitor/channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel

Table 1: The synthesis of the AGET requirements.

The design of the chip, additional simulations and global studies have pushed us to modify some items in the AGET requirements (for example the number of channels: 64 instead of 72). This will be explained in the following chapters.

2. Architecture of the front-end part of the channel

The architecture of the front-end part has been optimized to match the noise requirements for the TPC and to deliver a shaped signal making possible to perform a precise TPC drift-time measurement. It takes into account the power consumption and silicon area constraints and can also fit various configurations of detector parameters (gain, capacitor and drift velocity…), and can deal with the both detector signal (positive or negative) polarities.

2.1 General description

The front-end channel (**Fig. 5**) is made up of four stages:

- C.S.A: Charge Sensitive Amplifier,
- PZC: the pole-zero cancellation stage,
- R.C^2 filter: Sallen&Key filter,
- An inverting x2 Gain.

The parameters of the different stages are controlled by slow control, locally (at the channel level) or globally (at the ASIC level).

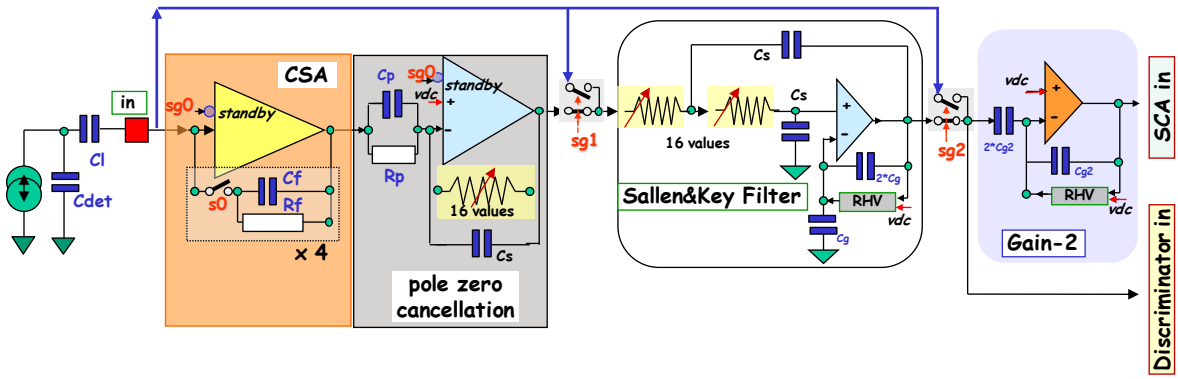


Fig. 5: Schematic of the front-end part of the analog channel.

The power supply, DC voltage and current references of the different stages are independent at the channel level and also at the ASIC level excepted for the inverting 2xgain and the discriminator.

2.1.1 Channel input

In the nominal mode, the input signal goes through the input of the CSA (Charge Sensitive Amplifier). But by slow control (state1<31:30>), it is possible to switch the signal to the input of the SK filter or inverting 2 x Gain (**Fig. 5**). In this case, the internal supply of the CSA and PZC filter will be cut off.

2.1.2 Charge Sensitive Amplifier (CSA)

This amplifier is based on single-ended folded cascode architecture. The input transistor is a NMOS device and its drain current is defined and controlled on ***Asad*** through the pad **126** or **155**. It is optionally possible to increase this current by a factor of 2 via the slow control (state1<0>). This bias current choice (max 1mA) will be the result

of a trade-off between the noise and power consumption performances that will depend on the application. It is also important to put additional decoupling capacitors to filter inside the chip the drain current bias to minimize the effect of the saturated channel on the neighbor channels. These pins are the 17, 34, 87 & 104.

The CSA DC output voltage is defined internally and must be filtered externally through the pads **133** & **148**. This DC value must be adapted, by slow control (state1<16>), to the polarity of the input signal. For the anode polarity (negative input current) 1.8V and 2.8 V for the other input polarity. The linear range of the CSA output voltage is **+/- 1 V**. The charge to voltage conversion is achieved by one of the four feedback capacitors selected by Slow Control. Their values are: **120 fF**, **240 fF**, **1 pF** and **10 pF** which are defining the four "ranges" of the chip (120 fC, 240 fC, 1 pC and 10 pC). This gain control is done channel by channel with two 64-bit slow control register state6<63:0> & state7<63:0> (2 bits per channel).

The DC feedback of the CSA is achieved by an attenuating current conveyor (AICON). It is equivalent to a resistor (**Fig. 6**) and there are 4 possible values, each associated with one of the feedback capacitor to obtain a fixed time constant value of 50 μs. This current conveyor attenuates by a factor A the current flowing through the Ra resistor connected between the CSA output and the AICON input, so that it is equivalent to a resistor of value Ax(Ra + Rin), where Rin is the AICON input impedance.

The maximum current that the CSA DC-feedback can source or sink to the detector is 5nA.

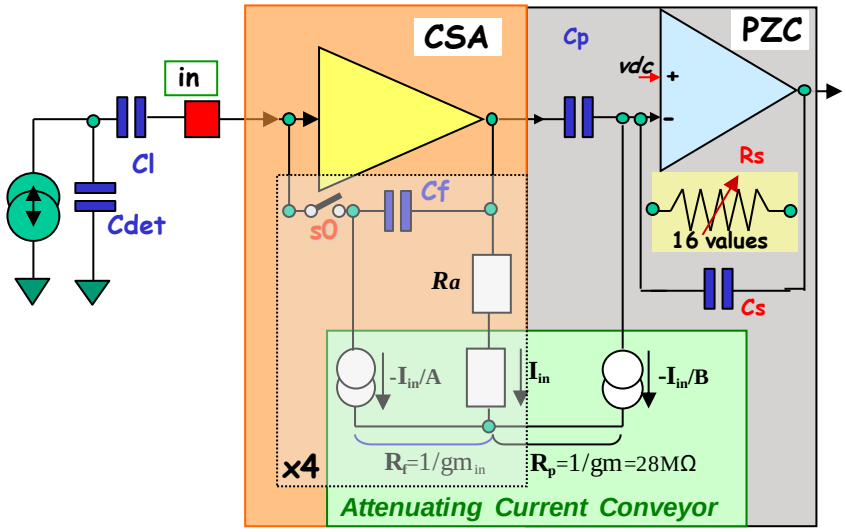


Fig. 6: **Principle of the CSA DC feedback.**

2.1.3 Pole-Zero cancellation stage (PZC)

The PZC stage is used to avoid long duration undershoots at the shaped output. It introduces a zero to cancel the low frequency pole of the CSA and replaces it by a higher frequency pole. Its value is selectable, via Slow Control (state1<6:3>), between sixteen possible values (25 ns to 0.5 μs).

The second branch of the CSA AICON (**Fig. 6**) is used to emulate the high value resistor (Rp) placed in parallel with the Cp to create a transmission zero cancelling the CSA pole. It is replaced by a new pole RsxCs defined by the feedback network of the stage that participates to the shaping.

The DC output voltage of this block is defined internally and must be filtered externally through the pads **134** & **147**. This d.c value must be adapted, by slow control (state1<16>), to the polarity of the input signal. For the anode polarity (negative input current) 2.2 V and 0.7 V for the other input polarity.

In the normal mode, the peaking time of the PZC and SK filter is the same and is controlled by the state1<6:3>. But it is possible to dissociate it to obtain a configuration near to an "integrator" mode. If the state1<9> is put to "1", the shaping time of the PZC will be fixed to 500 ns independently of the 16 possible shaping time values of the SK filter.

2.1.4 RC^2 filter (SK filter)

Associated with the previous PZC stage, this 2-complex pole Sallen-Key low pass filter provides a semi-Gaussian shaping of the analog channel. The filter damping factor is $\xi = 0.75$, so that the global filter response exhibits a 1% only undershoot.

The peaking time of the global filter is defined by switching different combination of resistors on both the PZC and SK filter stages. The available range of peaking time extends from **50 ns** to **1 μs** (**sixteen values**). The DC output voltage of the filter is defined internally as for the PZC (pads **134** & **147**).

2.1.5 Inverting x2 Gain (G-2)

This stage provides an extra x2 inverting voltage gain and the necessary buffering for the signal sampling in the SCA. Its total output dynamic (full range) is 1.5V, mainly limited by slew rate effects.

The DC output voltage of this block is defined internally and must be filtered externally through the pads **135** & **146**. This DC value must be adapted, by slow control (state1<16>), to the polarity of the input signal. For the anode polarity (negative input current) 0.7 V and 2.2 V for the other input polarity.

Its input common-mode voltage is defined internally and must be filtered externally through the pads **138** & **142**. These 2 pins are also used to supply the reference voltage of the SCA at a fixed value of 0.7V.

2.2 Architecture of the Fixed Pattern Noise channel (FPN channel)

A part of the SCA noise will be probably coherent between channels. To perform common mode rejection, 4 extra channels FPN (Fixed Pattern Noise) are included in the chip. The front-end part of these channels (**Fig. 7**) only includes the inverting 2x Gain stage where the inputs are connected to the input reference voltage. The F.P.N channels will be treated by the SCA exactly as the other channels. Off-line, their outputs can be subtracted from the other 64 analog channels. This pseudo-differential operation can reject the common noise due to 2x Gain and SCA i.e. clock feed-through and substrate coupling. It also improves the power supply rejection ratio (PSRR) of the chip. These channels are distributed uniformly in the chip as shown on **Fig. 30**. Their readout indexes are: 12, 23, 46 & 57.

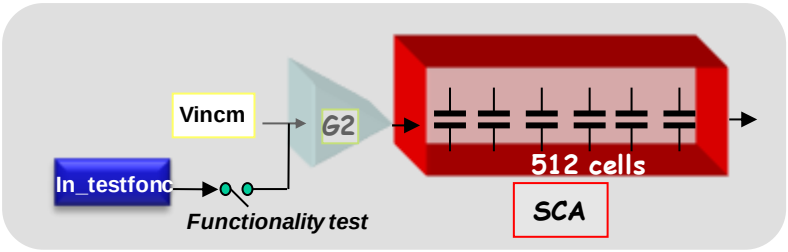


Fig. 7: Schematic of a FPN channel.

The FPN channels can be tested only by using the functionality test. In this case, the input voltage step from the In_testfonc input (pad n° 40) is applied directly to the input of the inverting 2x GAIN stage of the selected FPN channel.

3. Architecture of the event detection

The trigger signal (or “multiplicity” signal) is an important feature for the AGET ASIC, since it signals that an event has been detected.

The detection is made on the channel level by comparing the amplitude of the shaped signal (**Fig. 8**) with a programmable threshold value. The ASIC trigger signal has also the property to be not a logical signal (two levels: “0” or “1”) but an analog signal whit an amplitude proportional to the number of hit channels (64 possible values).

To improve the readout time, the channel trigger signal memorized in the hit register can be used as an address for the read out of its SCA memory.

The threshold channel integrates a differential buffer, a discriminator, a 7-bit DAC for the threshold and a memory register.

The output signal of the common filter (**Fig. 8**) is amplified through a differential buffer to cover an input dynamic range of the discriminator. This range can be fixed to 5% or 17.5% of input dynamic range of the analog channel. The differential gain is controlled by the bit state2<24>.

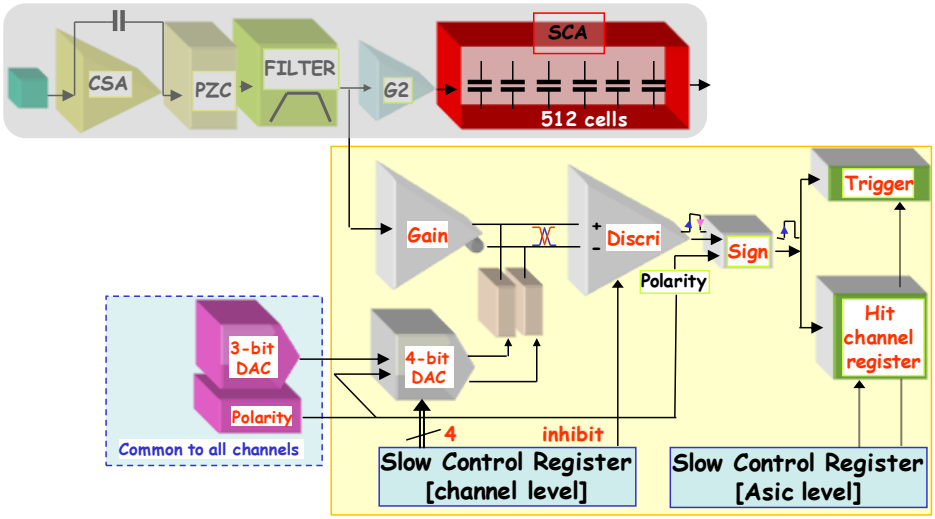


Fig. 8: block schematic of the channel.

The threshold value of the discriminator is controlled and adjusted through 2 DACs. The first is global to all the channels. Its 3 bits give the MSB of the threshold value plus 1 bit for polarity (state1<22:19>). The second is attached to the channel and its 4 bits (4 bits of state8<127:0> or state9<127:0>) give the LSB of the threshold.

If the signal cross the threshold, the discriminator output signal set the hit channel register to an active level and form with the 63 others discriminator signals a trigger signal.

The polarity bit is necessary to control the threshold and the logical output edge according to the polarity of the detector signal.

3.1 "Trigger" building at the channel level

The output signal of the discriminator gives the trigger signal under several conditions which are controlled by the slow control and some signals. This trigger signal switches a DC current source (**Fig. 9**) which is collected with the 63 others current sources to form the internal global trigger.

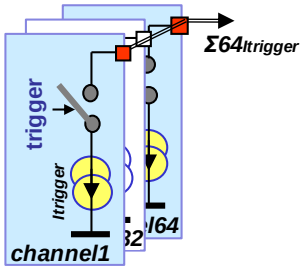


Fig. 9: block schematic of the channel trigger data.

3.1.1 Inhibition

There are 2 modes of trigger inhibition:

- The first mode is to disable the discriminator by putting it in a standby mode. In this case, neither trigger signal nor hit register data will be available at the channel level.
- The second is to disable only the trigger signal of the channel and to keep the functionality of the hit channel register.

These modes are controlled by 2 bits of slow control at channel level, coming from a 64-bit register of address 10 or 11 according to the channel number (see 9.7.K & 9.7.l).

3.1.2 Veto condition

It is also possible to suppress multiple consecutive triggers at the channel level during a time window, by introducing a veto condition. There are 3 possibilities:

- any veto,
- a fixed veto value of 4 µs [analog ramp generator & comparator],
- a veto given by the hit-channel register signal ("temporary register").

These veto conditions are controlled by the state1<24:23>.

3.1.3 Synchronization

The output signal of the discriminator can be sampled on the rising edge of the clock of the SCA sampling, and therefore the output trigger signal will be synchronous on this signal. This mode is controlled by the state1<25>.

3.1.4 Width of the signal

The width of the trigger signal can be:

- The same of the one of discriminator output signal (Time over Threshold). This mode is controlled by the state1<26>.
- Equal to two possible values: 100ns or 200ns. The choice is made by the state1<27> and enabled by the previous state1<26>=”0”.

These values are obtained by using mono-stable, and therefore are dependent of the process corners. The 2 slow control bits state1<29:28> will allow the control of these values (table 2).

State1<29> Msb_trigg_width	State1<28> Lsb_trigg_width	Range_trigg_width=”0”			Range_trigg_width=”1”		
		wp	tm	ws	wp	tm	ws
0	0	*61 ns*	*94 ns*	*128 ns*	*142 ns*	*218 ns*	*297 ns*
0	1	*50 ns*	*77 ns*	*106 ns*	*110 ns*	*170 ns*	*232 ns*
1	0	*72 ns*	*110 ns*	*150 ns*	*153 ns*	*235 ns*	*319 ns*
1	1	*83 ns*	*127 ns*	*171 ns*	*194 ns*	*298 ns*	*404 ns*

Table 2: the adjustment of the trigger width.

[wp for worst power case; tm for typical mean case; ws for worst speed case].

3.2 “Trigger” building at the asic level

The trigger signal at the ASIC level is formed by current to voltage conversion of the analog sum of 64 channel DC current sources (**Fig. 10**). The readout of this signal is controlled by slow control through several modes.

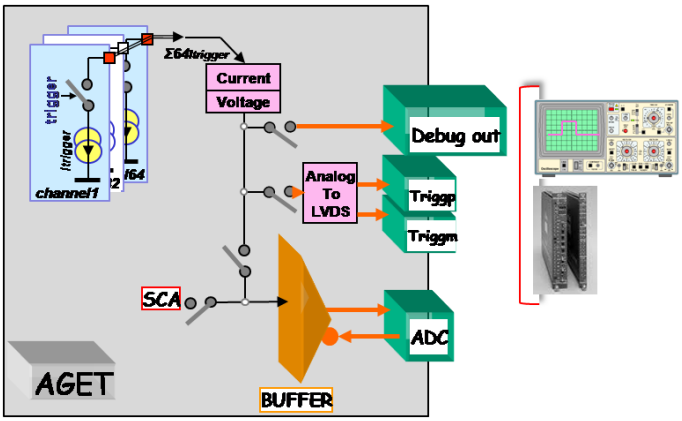


Fig. 10: block schematic of the AGET trigger data.

3.2.1 Disable of the trigger signal readout

By default, the readout of the trigger is done through the output buffer of the chip during the SCA sampling phase. But with the bit state2<20>, it is possible to disable its readout.

3.2.2 Other ways to readout the trigger signal

The readout of the trigger is done through the output buffer of the chip. For the test purpose, there is two another ways to readout this signal by using:

- Spy mode: The selection of the signal (1 among 6) is made with the 3 bits state2<2:0>. The readout of the signal is done through the pin Out_debug (pin n°46).

State2<2> Debug2	State2<1> Debug1	State2<0> Debug0	Out_debug (canal1)
0	0	0	*Standby*
0	0	1	*CSA*
0	1	0	*CR*
0	1	1	*Gain-2*
1	0	0	*Positive input of the discriminator*
1	0	1	*negative input of the discriminator*
1	1	0	*trigger*
1	1	1	*none*

Table 3: Selection of the output in the "spy" mode.

- The readout of the trigger is done through the pin Triggp (pin n°86) and pin Triggm (pin n°85) in LVDS levels. The output is enable by the state2<22> bit.

3.3 The hit channel register

The hit channel register allows the acquisition board to know if a channel has an event data stored in its SCA. This data will be taken as an address for the channel readout, if a selective readout is chosen.

3.3.1 Hit channel register architecture

The output signal of the discriminator sets a temporary register during a specific time (**Fig. 11**). On the falling edge of the SCA_write signal, the output of this register is stored in a register called "hit channel" register. The content of this register is used as an address for the readout of the channel's SCA analog data. With the "address channel control", this register's content can be read and even changed by a write operation, just before the SCA readout.

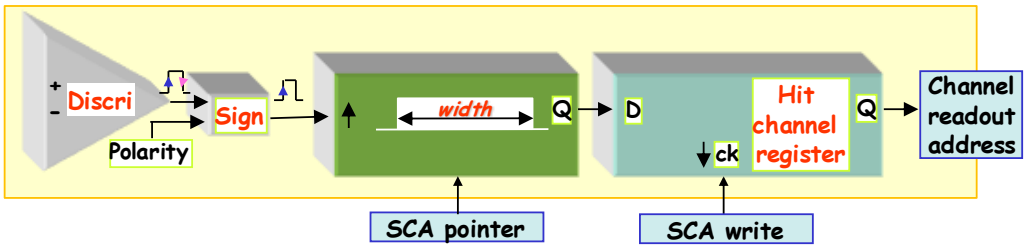


Fig. 11: The architecture of hit channel register.

3.3.2 Memory time before validation in the hit channel register

As the trigger signal has a limited time width, it is necessary therefore to store its state in a register, called "temporary" register. If the signal detection at the ASIC level (trigger signal) is considered as a good event, the SCA sampling is stopped. The "temporary" register content is stored in a final register called "hit channel" register, on the falling edge of the SCA write signal.

But in the case where the event is rejected, the system doesn't interrupt the SCA sampling and therefore a SCA write signal remains in the same state. So as the temporary register must be cleared, the memory time in this register is in fact defined by using the SCA address pointer (**Fig. 12**).

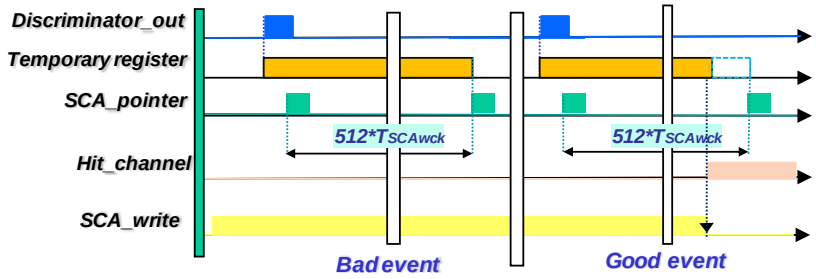


Fig. 12: The memory time operation.

This memory time is fixed to a value corresponding to the sampling time of all the memory or a part of the memory according to the state1<11:10> bits.

State1<11> Pointer 1	State1<10> Pointer 0	SCA pointer address
0	0	*Column 0*
0	1	*Column 0 or 256*
1	0	*Column 0, 128, 256 or 384*
1	1	*Any SCA pointer address*

Table 4: Definition of the SCA pointer address.

The first configuration (00) corresponds to the nominal configuration (SCA of 512 cells) and the second (01) for the 2p decay case (2 SCA of 256 cells). The third configuration (10) can be used for complex events. The last configuration (11) gives a continuous memory time (the trigger is stored until the end of the SCA sampling).

3.3.3 Case of two consecutive events

If a second event arrives when the temporary register is busy, the time of memory will be increase by one complete SCA writing phase (**Fig. 13**).

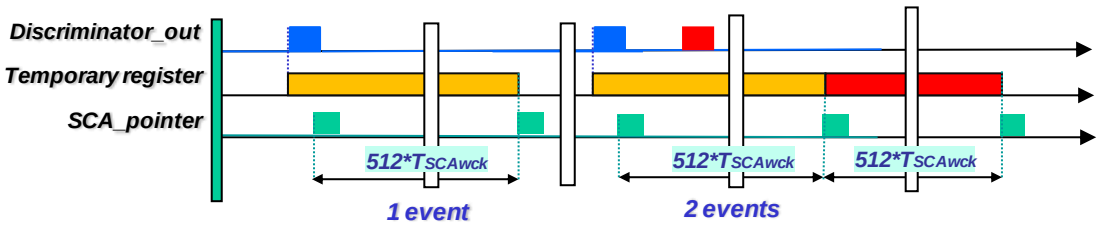


Fig. 13: The two events operation.

This feature is useful in the case where the first event is rejected and the second is considered as good event.

4. Channel address access

The AGET chip offers the possibility to read only the hit channels or some specific channels. To do this, it is necessary to access the internal hit register (1 or 2 per channel according to the di-protons mode) where the hit channel data is stored and used during the SCA readout phase to select the analog data of the channel.

The access to the hit channel register uses the same link of the Slow Control. The protocol frequency foreseen is 50 MHz.

4.1 Write phase [writing of the read channel address]

The write phase (**Fig. 14**) is defined by the first bit **r/wb = 0** on ***Sc_din***. The next bits correspond to the address of the selected channels. The data format is as follow: channel 1 to 68 (channel 1 to 34 in the 32 channels mode).

The ***Sc-en*** signal must frame all the data bits (write bit + 68 or 34 bits), and a minimum of 1 pulse of ***Sc_ck*** after the falling edge of ***Sc_en*** is necessary to finish the write phase (the effective write operation of the data in the register is made on the next rising edge of the ***Sc_ck*** after the falling edge of ***Sc_en)***.

During the write phase, ***Sc_dout*** takes the states of the hit channel registers, according to the history, then comes back to its high impedance state (HZ) after the falling of ***Sc_en.***

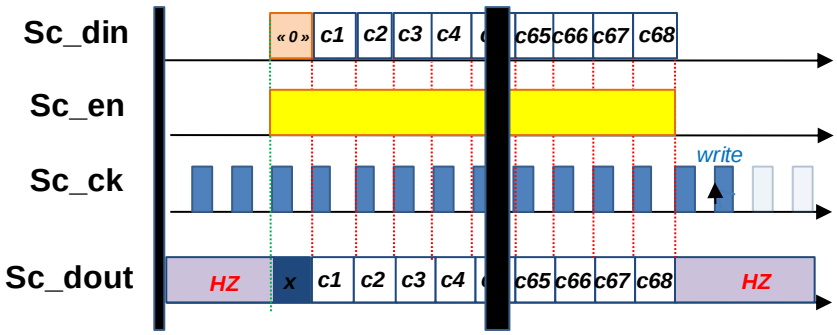


Fig. 14: The writing phase operation.

4.2 Read phase [read of the hit channel register]

The read phase (**Fig. 15**) is defined by the first bit **r/wb = 1** on ***Sc_din***. On the next rising edge of the ***Sc_ck***, the data of the hit register are put on the ***Sc-dout***. The data format is as follow: a first bit corresponds to the address of the memory register range ("1" for Mem1to256or512, "0" for Mem257to512) and the next for the channel hit registers 1 to 68 (or channel 1 to 34 in the 32 channels mode).

The ***Sc-en*** signal must frame all the data bits (70 or 36 bits), and the ***Sc_ck*** can be stopped.

The ***Sc_dout*** goes back to its high impedance state (HZ) after the falling of ***Sc_en.***

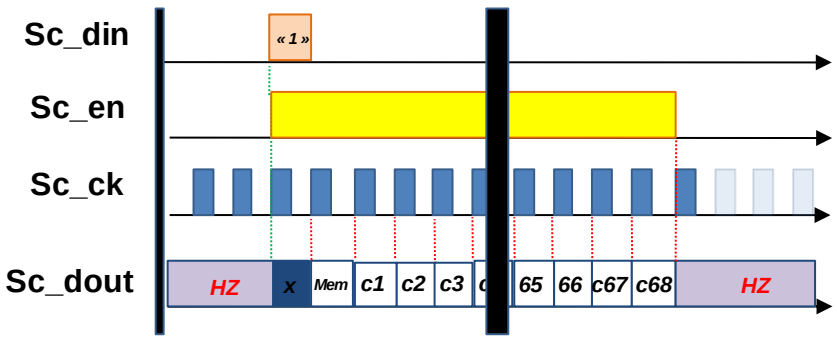


Fig. 15: The read mode operation.

5. The 2p decay case

The typical event (implantation & decay) studied by the CENBG team, implies to split the SCA in two separate memories of 256 cells. This configuration is programmable by the state1<12> bit.

Register N°	Bit N°	Name	Action
1	12	*SCA splitting*	*"0": I memory of 512 cells; "1": 2 memories of 256 cells*

To optimize the channel readout, there is two hit channel registers per channel. One, if the SCA depth is equal to 512 memory cells, or two if the SCA is split in two x 256 memory cells. In the 2p decay, each hit channel register is associated to one bank of memory, working in different modes.

5.1 Description of the SCA write and SCA & hit register read phases

In the nominal configuration (1 SCA memory of 512 cells), the memory of the trigger in the hit channel register is made at the end of the SCA write phase (falling edge of the Write signal). The readout (write) of this register data can be performed by the channel address control process before the SCA readout phase (before the rising edge of the Read signal).

In the 2p decay, the previous process will be used (**Fig. 16**) for each memory bank. Two first separate phases of SCA write where each of the 2 two bank of memories will be in sampling phase (the other not) with its hit register enabled (the other not). The two last phases where for each of the memory the hit register will be readout or write firstly before the analog memory readout.

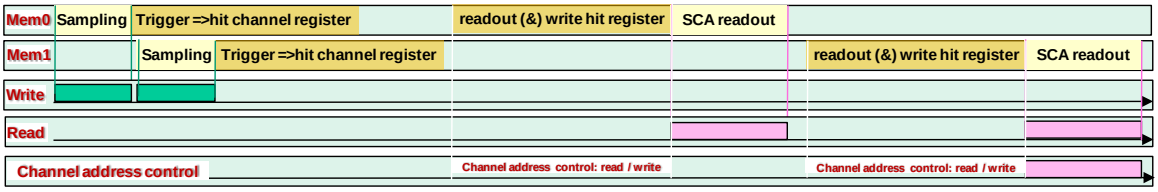


Fig. 16: The chronogram of the signal processing in the 2p decay case.

5.2 The initialization phase

After a power on phase or a number of acquisition cycles, it is important to define at the AGET level which will be the first memory bank in the sampling mode (and readout mode). By definition, the first memory is the mem0 and the second mem1. This is done, if during an active state of the Write SCA signal, there is only one rising edge of the SCA write clock (**Fig. 17**).

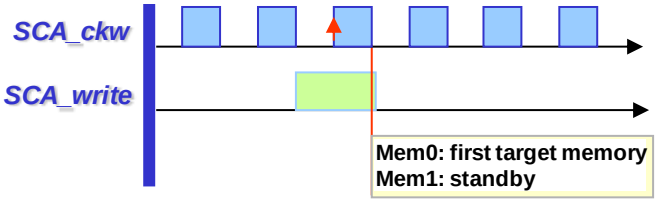


Fig. 17: The initialization phase.

5.3 The sampling phase

The sampling phase of each memory is defined, firstly by the initialization phase, and after on each falling edge of the SCA write signal. The internal logic of AGET will switch automatically from one memory to the other if the SCA-write signal is interrupt between one or two rising edge of the SCA write clock (**Fig. 18**). A latency time of 3 clock periods is necessary before the effective change.

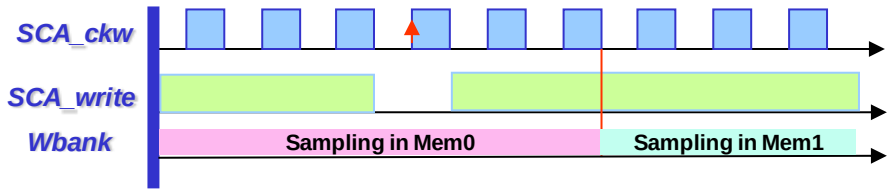


Fig. 18: Selection of the memory bank number in SCA sampling phase.

5.4 The readout (&) write phase of the hit register

After the sampling phase of each memory (**Fig. 18**), the readout of the hit register of the two memories must be done, and can be also followed by a written task. In first, the memory selected is the mem0 until the falling edge of the SCA read signal (**Fig. 19**). A latency time of 6 clock periods is necessary before the effective change.

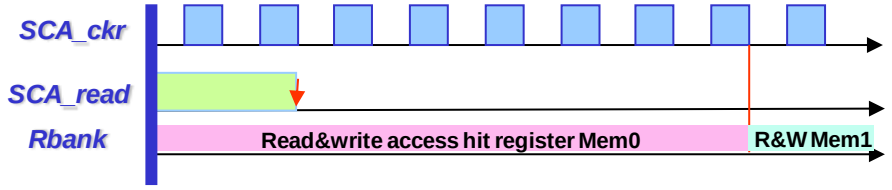


Fig. 19: Selection of the memory bank number in the readout & write phase.

6. Architecture of the SCA

The analog memory is based on the **S**witched **C**apacitor **A**rray structure. It is used as a 512 cell-depth circular buffer in which the analog signal coming out from the front-end analog channel is continuously sampled and stored at a sampling frequency rate. The sampler is stopped on the trailing edge of the **Write** signal of the chip. Then all or one part of the 512 samples of each or selected channels are read back. The output analog data is time-domain multiplexed then fed toward a single external 12-bit ADC channel.

6.1 General description

Each one of the 68 channels has 512 switched capacitor cells, which are arranged in line. All the capacitors of a line are sharing the same input analogue and reference busses and the same read top and bottom busses connected to a read amplifier. All the cells of the 68 channels with the same index (namely a column) are sharing the same write and read column signals. It means that all the cells of a column are written or read at the same time. The write and read operations are performed successively.

6.2 Description of the Write and Read SCA operations

The SCA uses 4 digital command signals.

- Two clocks sequencing the write and read operations:
- **Wck** : the write clock;
- **Rck** : the read clock.

These clocks are active on their rising edges, and may be interrupted when they are not used.

- Two frame signals defining the write and read operations (**Fig. 20**):
- **Write**: defining the write operation;
- **Read**: defining the read operation.

These two signals should not overlap and are active on their high levels. The clock signals are provided using differential LVDS levels. The write and read signals are received in CMOS levels.

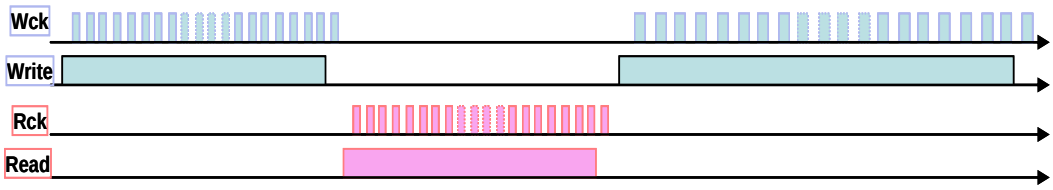


Fig. 20: Definition of the SCA write and read phases.

6.2.1 The SCA write phase

The write operation starts when the ***Write*** signal is set to 1. Its positive edge asynchronously resets the write pointer to column 0 of the SCA. This pointer is incremented on the next rising edge of ***Wck***, performing the writing operation. When ***Write*** comes back to 0, the write pointer position is frozen and the writing operation is stopped.

The ***Write*** signal can be set or reset asynchronously with the clock, but in this case the write operation on the last cell may be incomplete. So it is better to change the state of the ***Write*** signal on the falling edge of ***Wck.***

To complete the write operation, at least one ***Wck*** rising edge is required after the ***Write*** signal falling edge.

6.2.2 The SCA read phase

The read operation is initiated when the ***Read*** signal is set to “1”. Its positive edge asynchronously copies the write pointer to the read pointer. As long as Read stays “1”, the analog signals are sequentially multiplexed to the output at each ***Rck*** rising edge. The first column which is read is the one following the previous for which the SCA write operation has been stopped, with a programmable offset (0 to 511) setting by the state12<15:0>.

The readout channel number will depend on the mode chosen. According to the state1<14> bit, the number can be all channels or only the hit channel(s) or selected channels. The data format per column (**Fig. 21**) starts by a “reset” data follow by the analog data memorized in the cell of the selected channels. The “reset” signal should take into account the settling times of the column multiplexors and buffers. The width of the “reset“ signal can be equal to 4 or 2 ***Rck*** according to the state2<19> bit.

After the last cell of the column, the read pointer is shifted and the same operation is performed on the next column**.**

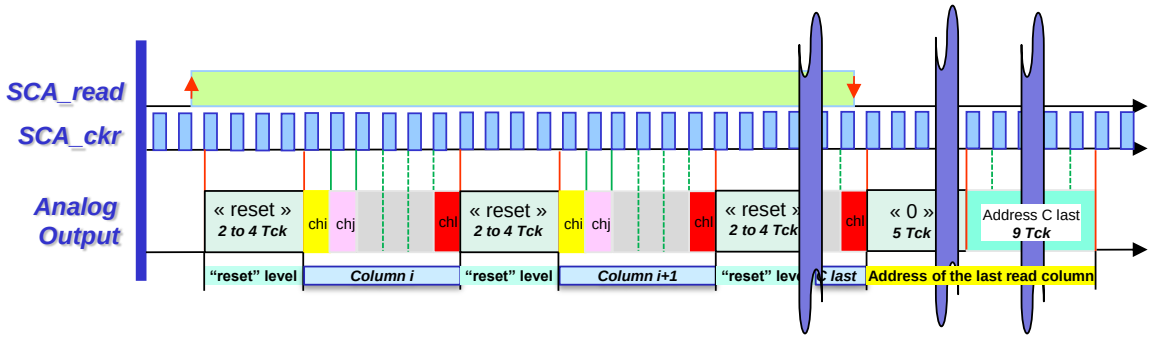


Fig. 21: Chronogram of the SCA Read phase.

When ***Read*** comes back to 0, this sequence is asynchronously interrupted and the current address of the read pointer is encoded and multiplexed to the output. An asynchronous ***Read*** signal allows the user to read a specific number of cells instead of all cells. Note that, by setting ***Write*** to 1 the readout process is halted regardless of what Read is set to.

As for Write, it could be convenient to set or reset the ***Read*** signal on the negative edge of ***Rck***.

6.3 Reading the last read cell index

After the ***READ*** signal comes back to 0, a special frame, coding the physical index of the last read cell, is sent out. This serial frame uses binary levels which are clamped internally in the chip by the multiplexer and the output buffer. To recover the digital levels, the user shall keep the state of the ADC's MSB only.

The special frame is constructed as follows:

- 5 binary low levels.
- 9 bits coding the last read cell index sent serially (MSB first).

At the end of this operation, the analogue output comes back to the reset level.

The last read cell information can be used to check the synchronization between SCA chips or to correct data from physical fix pattern noise (i.e. pedestal dependency with the physical index of the SCA cell).

If the state2<4> bit is set to 1, the control word "101011001" is sent instead the last read cell address for debugging purpose.

6.4 The power on phase

After a power on, the state machine used for the SCA readout can be in an indeterminate state. To initialize this state machine, it is necessary to send a SCA read signal with a width equal to 3 periods of the SCA read clock signal (**Fig. 22**). This kind of signal can eventually be sent in the case where the SCA readout is abnormally interrupted.

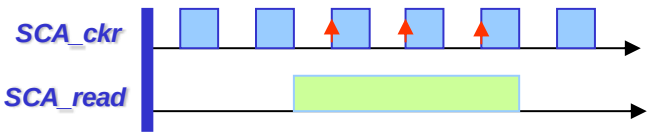


Fig 22: SCA readout state machine reset.

7. The differential output buffer

This buffer is designed to differentially drive the external 12-bit ADC at up to 25 MHz readout frequency. Its input, connected to the SCA multiplexer output, is single-ended while its output is differential. As shown on **Fig. 23**, the single-ended to differential conversion is achieved using a full differential amplifier with its negative input connected to a reference voltage **Vicm** This buffer also provides a gain of 1.328 between the differential output (V_{op}-V_{on}) and its input (V_{ip}) to fit with the differential ADC input range (**+/-1 V**). Thanks to an internal common mode feedback, the common mode output voltage of the amplifier ((V_{op}+V_{on})/2) is equal to the voltage applied on the ***vocm*** (Pin **68**) input. Its value can be fixed between 1.5V and 1.65V.

The common mode input voltage (**Vicm**) is defined internally and must be filtered externally through the pad **71**. The value of this voltage is controlled by the state1<18:17> bit, to take into account the signal polarity and the offset voltage.

The buffer has to deal with the ADC input architecture and the parasitic elements due to interconnection on the ***Asad.*** It is designed to have a settling time smaller than 20 ns corresponding to half the ADC clock period.

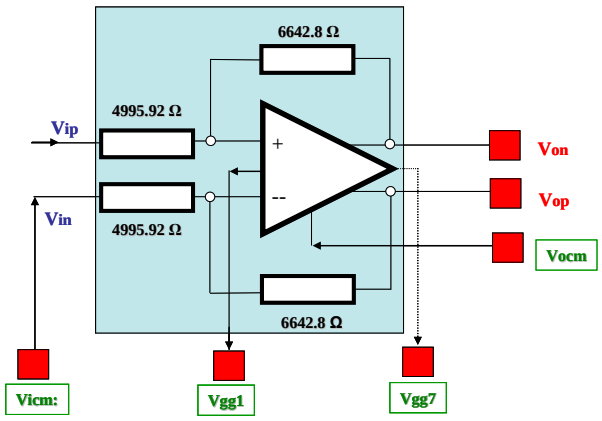


Fig. 23: Schematic of the readout buffer.

This settling time can be optimized by adjusting externally the current Vgg7 of the output stage (pad **70**).

8. Architecture of the test & “spy” mode systems

The AGET chip includes a test system useful for the electrical calibration, ASIC test bench and functionality control of all electronic channels (ASIC to acquisition board). The chip also offers the possibility to spy on 4 critical signals of the front-end part of channel#1: CSA output, PZC output, Gain-2 output and discriminator inputs or the ”multiplicity” signal.

8.1 General description of the TEST SYSTEM

The AGET ASIC offers 3 different test modes: calibration, test and functionality.

The Calibration operation consists of generating the same charge on the inputs of all channels of all ASICs of a given Asad or all Asads of a detector readout plan. Therefore, the charge pulse is generated outside of the chip, i.e. on the Asad (**Fig. 24**).

The charge injection is generated by applying a step voltage to a precision capacitor connected to the input of the selected channel via the ***In_cal*** input (pin **39**).

The channels selected are configured by slow control (state3<33:0> or state4<33:0>).

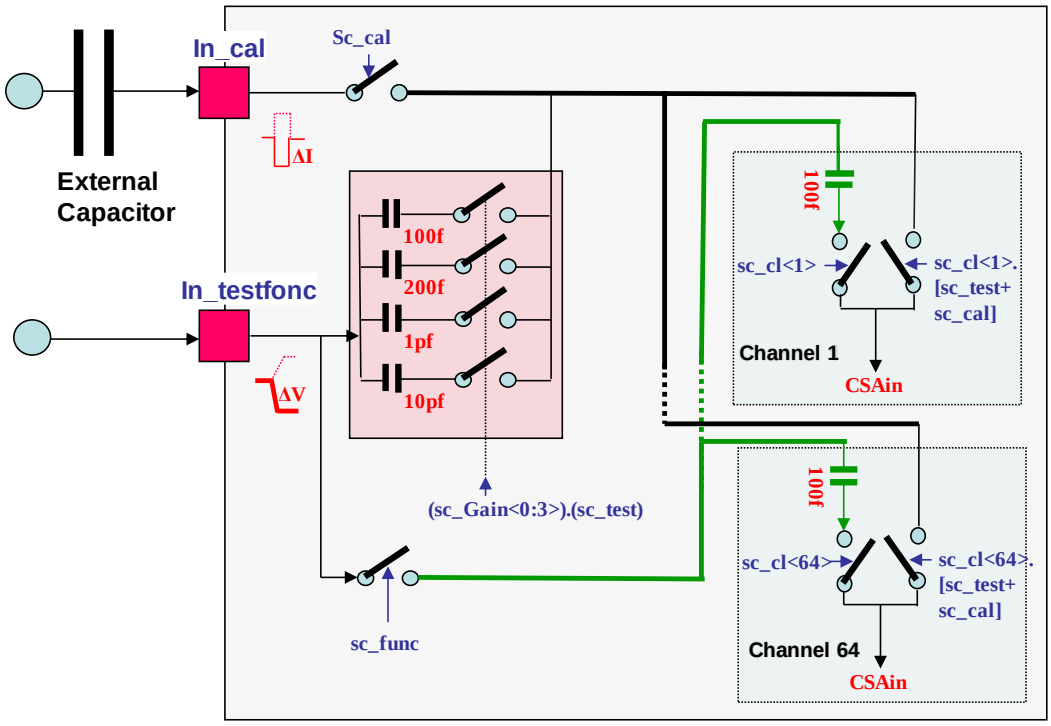


Fig. 24: Schematic of the test system.

For the two other modes, the charge injection is generated through internal capacitors driven by an externally generated voltage applied on the pad ***In_testfonc*** (pin **40**).

In the test mode, four different values of injection capacitor, one for each charge range, are used. This permits working with the same test voltage pulse level for the 4 ranges. The selection of the injection capacitor is done with the state1<2:1> bits.

In the functionality test mode, a single capacitor (100 fF) per channel is used.

For all the 3 test modes, the selection of the tested channel is made via slow control. For the first two modes, i.e. calibration and test, only one tested channel must be selected whereas up to the 68 channels can be selected when the functionality mode is used. For the FPN channels, only the functionality test is usable.

8.2 General description of the "spy" mode system

This mode allows the user to view the outputs of CSA, PZC, Gain-2, the discriminator inputs of channel number 1 and the trigger signal on an oscilloscope (**Fig. 25**).

This feature will be useful to compare experimental and simulation results. By the state2<2:0> bits, one of these signals can be multiplexed, through an internal buffer, to the pad ***Out_debug*** (pin 46).

If the "spy" mode is not selected, the internal buffer is put in a standby mode.

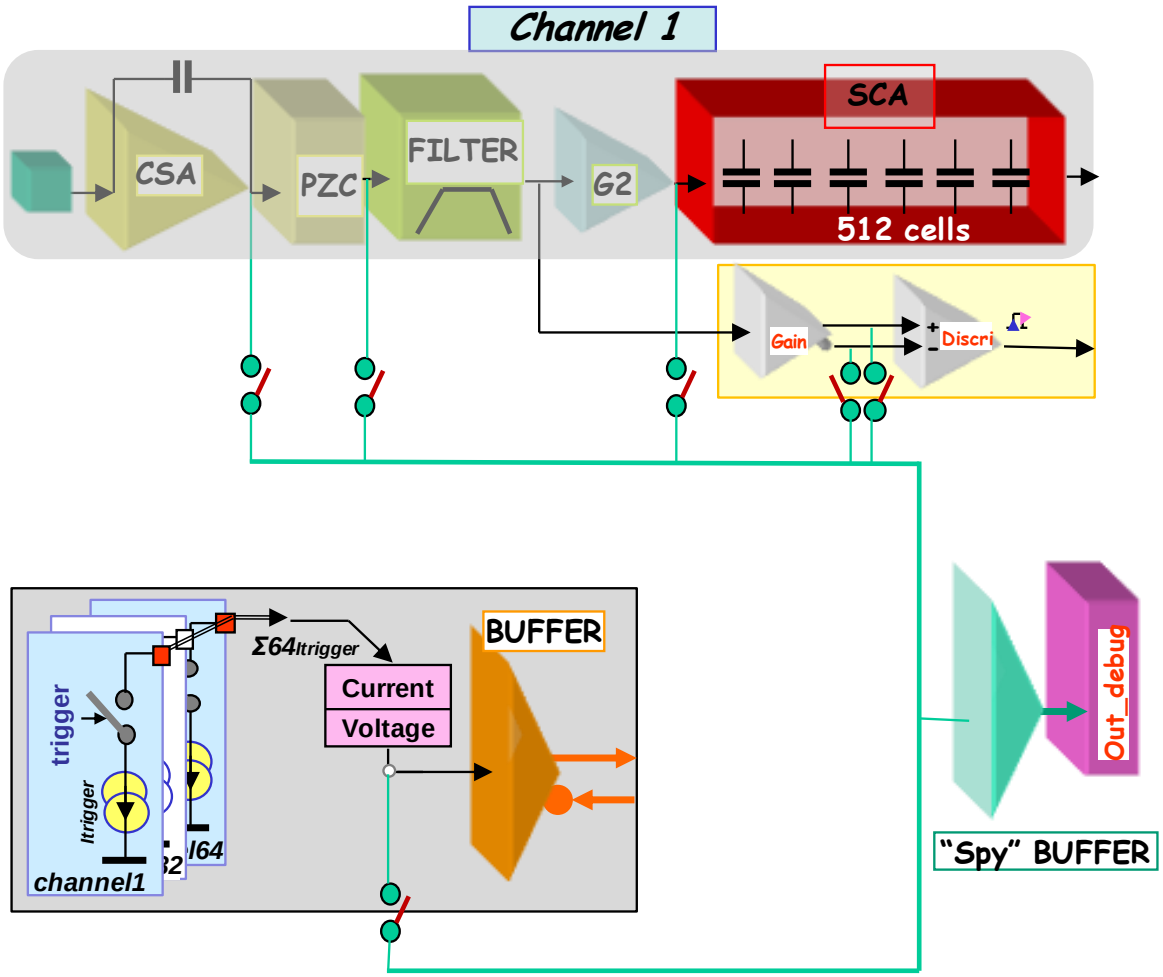


Fig. 25: Schematic of the "spy" system.

9. The AGET slow control

The slow control permits the user to program various chip parameters (gain, shaping time, test mode, etc) and to access specific modes of operation. “Slow Control” is a serial protocol which is used in several ASICs designed in IRFU laboratory. Here, it provides us with read/write access to 13 internal registers.

9.1 Power on Reset

When the chip is powered on, an internal “power on reset” device delivers a reset pulse (about 1ms of duration) resetting all the registers (all bits to 0), except for register 5 which is read only.

9.2 Description of the slow control protocol

Because we use the same link for the slow control and the channel address control, the 2 protocols are distinguished by the detection of specific data pattern on the ***Sc_en*** and ***Sc_din*** lines.

The slow control mode is enabled after 3 successive pulses on the ***Sc_en*** line and the ***Sc_din*** is set to the “1” level (**Fig. 26**).

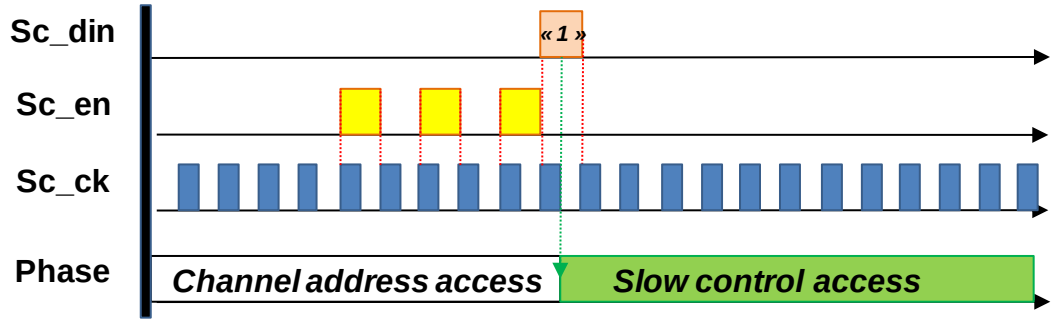


Fig. 26: Definition of the slow control mode.

The slow control mode is disabled if after 3 successive pulses on the ***Sc_en*** line and the ***Sc_din*** is set to the “0” level (**Fig. 27**).

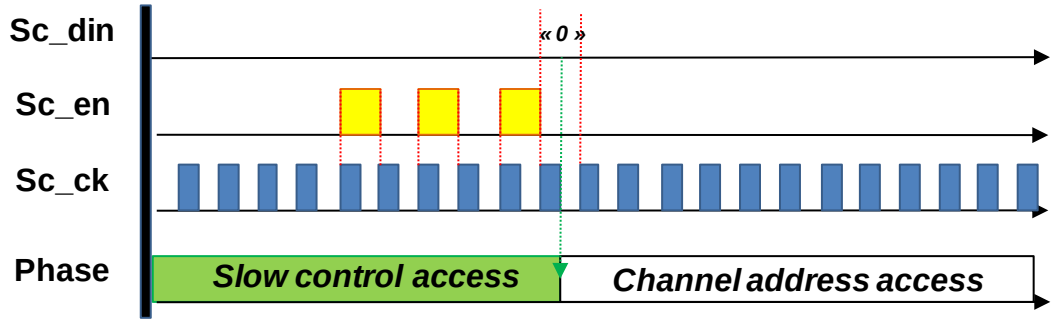


Fig. 27: Definition of the channel address control mode.

9.3 Description of the slow-control serial link

The link uses **4** signals [They all use **CMOS** [0V; 3.3V] standard]:

- ***Sc_din*** *[pin n°51]*: input data of the serial link.
- ***Sc_ck*** *[pin n°53]*: clock of the serial link.
- ***Sc_en*** *[pin n°52]*: enable of the serial link.
- ***Sc_dout*** *[pin n°54]*: output data of the serial link.

The signals ***Sc_din*** & ***Sc_en*** must be synchronous to the rising edge of ***Sc_ck.*** The data are sampled on the input lines, decoded and the operations of reading/writing are carried out, by the ASIC, on the falling edge of ***Sc_ck***. Thus, the data at the output of ***Sc_dout*** are synchronous on this edge.

On ***Sc_din,*** the data frame is defined as:

[**r/wb**] [**Ad6… Ad0**] [**DNBD-1…D0**]

[**r/wb**]: This first bit defines the type of operation. **r/wb** =1 : readout; 0: write.
[**Ad6… Ad0**]: These 7 bits give the address of the target register.
[**DNBD-1…D0**]: This is the **NBD** bits of data to transmit.

The most significant bit of the address and the data is always sent (or read) first.

The ***Sc_en*** signal frames the data sent on ***Sc_din***. It must go up simultaneously with the positioning of [**r/wb**] and must go down one cycle of ***Sc_ck*** after the positioning of the last bit of data (***D0***) on ***Sc_din***. Thus, the data packet defined by setting the ***Sc_en*** signal to 1 must frame [***8+ NBD*** falling edges**]** of ***Sc_ck***.

The ***Sc_ck*** clock must be present immediately after the beginning of the data frame and must continue at least during four clocks (falling edge) after the falling edge of ***Sc_en***. After that, it is better to stop it (its idle state can be high or low).

Between the slow-control frames, the ***Sc_dout*** output is in idle state. If the ***force_eout*** bit of the register 2 is high, this output keeps its last valid value. If it is low (default mode), the output is in high impedance state.

9.4 Resynchronization of Sc-dout

All the data on the ***Sc_dout*** line are, by default, locally synchronized on the ***Sc_ck*** falling edge. But this synchronizing is partially lost due to the different transit times in the chip. It is also possible, by slow control, to synchronize the signal on ***Sc_dout***. This is done by the bit 9 (***out_resync***) of the register 2, and the choice of active edge by the bit 10 (***synchro_inv***). That is if the state is “1”, the synchronization will be made on the falling edge of ***Sc_ck***; “0” on the rising edge. All the chronograms on the next figures are in the case where the slow control bit ***out_resync*** is “0”.

9.5 Write mode (address other that 0) in a register of NBD bits

The write mode (**Fig. 28**) is defined by the first bit **r/wb = 0** on ***Sc_din***. The falling edge of ***Sc_en*** starts the writing of the **NBD** last bits on ***Sc_din*** in the target register. After the eighth falling edge of ***Sc_ck***, ***Sc_dout*** leaves its idle state. During **NBD** clocks, ***Sc_dout*** takes the **Q0<n:1>** states, according to the history on the **Sc_din** line. Then, it will take the states present **NBD** clocks before (A<0>, D<NBD-1>, D<NBD-2> and D<NBD-3>).

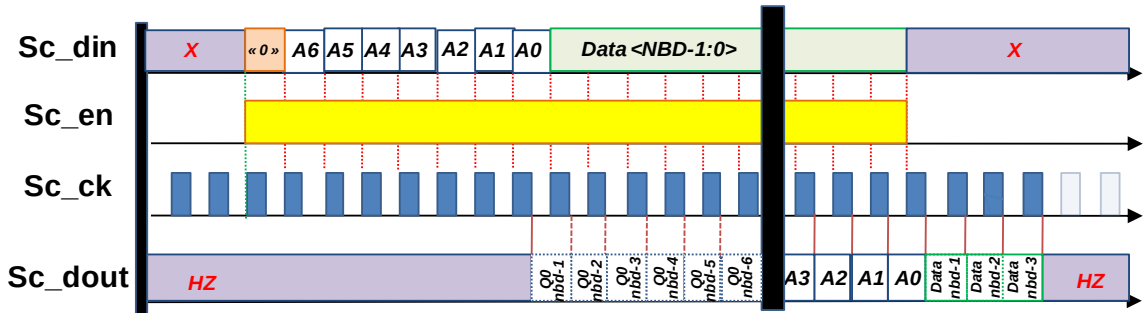


Fig. 28: The write mode.

Sc_dout will come back to its idle state 4 falling edges of the clock after the falling of ***Sc_en.*** The number of **NBD** bits present in the data part of ***Sc_din*** can be greater than the size of the register (**C** bits). In this case, only the **C** last bits will be written in the register. The **NBD-C-3** first bits of the data will go out on the ***Sc_dout*** after A0, DNBD-1, DNBD-2 & DNBD-3. This feature can be used to test the serial link.

9.6 Read operation on a NBD bits register

In the readout mode (**Fig. 29**), ***Sc_en*** must cover more than **8+NBD-2** falling edges of ***Sc_ck***. A minimum of 4 falling edges of ***Sc_ck*** after the falling of ***Sc_en***, is necessary to finish the reading phase.

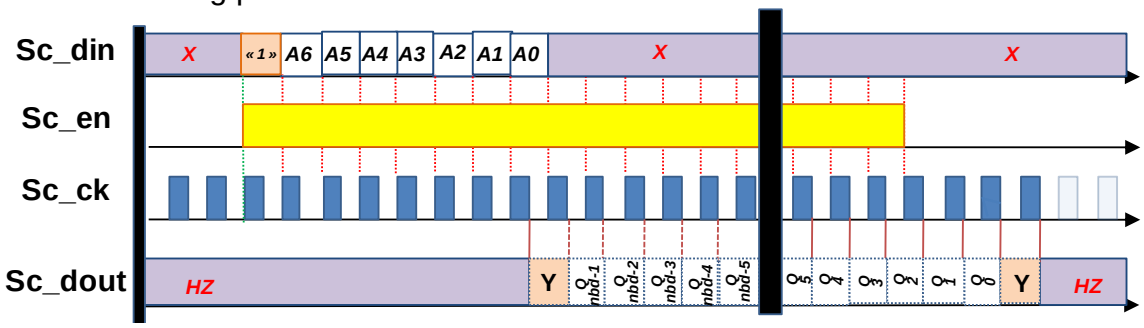


Fig. 29: The read mode.

The first bit on ***Sc_din*** must be to “1” (**r/wb).** Thus the 7 other bits define the address of the register. The next bits are ignored.

At the eighth falling edge of ***Sc_ck***, the address is decoded and ***Sc_dout*** leaves the idle state. At that point (first Y in the figure), the value of Sc_dout depends on the previous state of the serial link.

At the ninth falling edge of ***Sc_ck***, the data of the register is serialized out on ***Sc_dout*** for **NBD-1** clock cycles. After these **NBD** clock cycles, the data coming out from the ***Sc_dout*** are not valid.

9.7 Description of the slow control registers

The AGET chip includes 13 internal registers for the ASIC configuration shown in table 5.

address	name	width	access	action
0	**dummy**		W	serial link test purpose
1	**ASIC configuration 1**	32 bits	R/W	chip configuration
2	**ASIC configuration 2**	32 bits	R/W	Special modes and test configuration.
3	**First group test selection**	34 bits	R/W	selection of tested channels (1 to 32)
4	**Second group test selection**	34 bits	R/W	selection of tested channels (33 to 64)
5	**ASIC version number**	16 bits	R	Contains the version number of the chip
6	**Gain 1 to 32**	64 bits	R/W	Input charge range of the channel 1 to 32
7	**Gain 33 to 64**	64 bits	R/W	Input charge range of the channel 33 to 64
8	**threshold 1 to 32**	128 bits	R/W	threshold of the channel 1 to 32
9	**threshold 33 to 64**	128 bits	R/W	threshold of the channel 33 to 64
10	**Inhibition 1 to 32**	64 bits	R/W	inhibition of the channel 1 to 32
11	**inhibition 33 to 64**	64 bits	R/W	inhibition of the channel 33 to 64
12	**Roffset**	16 bits	R/W	Offset for the SCA read.

Table 5: Mapping of the AGET slow control registers.

9.7.A Register 0

The register **0** doesn't physically exist. But, when it is addressed in write mode, ***Sc_dout*** recopies the data on ***Sc_din*** (after the eighth falling edge of ***Sc_ck***). ***Sc_dout*** comes back to the idle state (4 falling edges after the falling edge of ***Sc_en***).

9.7.B Register 1

This 32-bit register is located at address number 1 (table 6). This register controls the main configuration of the chip.

bit	name	action
0	**Icsa**	if 1, the nominal CSA bias current is x2
1	**Gain0**	LSB of the internal test capacitor in Test mode
2	**Gain1**	MSB of the internal test capacitor in Test mode
3	**Time0**	LSB of the filter peaking time
4	**Time1**	bit 1 of the filter peaking time
5	**Time2**	bit 2 of the filter peaking time
6	**Time3**	MSB of the filter peaking time
7	**Test0**	LSB of the test mode register
8	**Test1**	MSB of the test mode register
9	**Integrator mode**	If 1, set the PZC shaping time value to 500 ns
10	**SCA pointer 0**	LSB of the SCA pointer
11	**SCA pointer 1**	MSB of the SCA pointer
12	**SCA splitting**	If 1, the SCA is divided in two blocs of 256 cells
13	**32 channels mode**	If 1, the number of effective channel is 32 (group 1 to 32)
14	**Readout mode**	Specify the readout mode: "1": all channels; "0": hit or selected channels
15	**FPN readout**	If 1, the FPN channels are readout
16	**Polarity**	Specify the polarity of the input detector signal
17	**Vicm0**	LSB of the input common mode voltage of the data buffer
18	**Vicm1**	MSB of the input common mode voltage of the data buffer
19	**DAC 0**	LSB of the global threshold DAC
20	**DAC 1**	Bit 1 of the global threshold DAC
21	**DAC 2**	MSB of the global threshold DAC
22	**DAC sign**	Sign bit for the 64 channel threshold
23	**Trigger veto 0**	LSB of the trigger logic veto
24	**Trigger veto 1**	MSB of the trigger logic veto
25	**Synchro_discri**	if 1, discri out synchro of CKscaWrite (rising edge)
26	**tot**	if 1, width trigger = output discri (Time over Threshold)
27	**Range_trigg_width**	Select the width range of the trigger signal (100ns/200ns)
28	**Lsb_trigg_width**	LSB of the trigger width & amplitude
29	**Msb_trigg_width**	MSB of the trigger width & amplitude
30	**External 0**	LSB of the external input selection
31	**External 1**	MSB of the external input selection

Table 6: Register 1.

This is the description of the different bits used to control and to configure the AGET circuit.

✓ ***state1<0>: Bit Icsa.***

This bit sets the current multiplier of the CSA input transistor, when set to 1 the current value is scaled by 2. This bit allows the user to optimize the power consumption or the noise resolution.

✓ ***state1<1:2>: Bit Gain0 to Gain1.***

These 2 bits select the internal test capacitor (table 7) in the ***test*** mode.

Gain1	Gain0	Capacitor Value
0	0	*120 fF*
0	1	*240 fF*
1	0	*1 pF*
1	1	*10 pF*

Table 7: Choice of the internal test capacitor.

✓ ***state1<3:6>: Bit Time0 to Time3.***

These 4 bits set the peaking time of the shaper (table 8), by switching resistors on the PZC & SK filters.

Time3	Time2	Time1	Time0	Peaking Time [5%_100%] (ns)
0	0	0	0	*69.67*
0	0	0	1	*117.3*
0	0	1	0	*232.3*
0	0	1	1	*279.7*
0	1	0	0	*333.9*
0	1	0	1	*382.7*
0	1	1	0	*501.8*
0	1	1	1	*541.3*
1	0	0	0	*568.2*
1	0	0	1	*632.5*
1	0	1	0	*720.9*
1	0	1	1	*760.3*
1	1	0	0	*830.7*
1	1	0	1	*869.2*
1	1	1	0	*976.5*
1	1	1	1	*1014*

Table 8: Definition of the peaking time.

✓ ***state1<7:8>: Bit Test0 to Test1.***

These bits define the test modes (table 9).

Test1	Test0	Test mode
0	0	*nothing*
0	1	*calibration*
1	0	*test*
1	1	*functionality*

Table 9: Definition of the test modes.

The **calibration, test & functionality** tests require selecting one or several channels. This is done by registers 3 & 4. For the **test** mode, it is also necessary to select the internal capacitor (Gain 0 & 1 of the register 1).

✓ ***state1<9>: Bit integrator mode.***

This bit fixes the shaping time of the PZC stage to 500 ns value independently of the 16 possible shaping time values of the Sallen-Key filter.

✓ ***state1<10:11>: Bit SCA pointer 0 to pointer 1.***

These two bits define the time marker of the SCA pointer pass. This marker defines the memory time of the trigger in the hit register (table 10).

Pointer 1	Pointer 0	SCA pointer address
0	0	*Column 0*
0	1	*Column 0 or 256*
1	0	*Column 0, 128, 256 or 384*
1	1	*Any SCA pointer*

Table 10: Definition of the SCA pointer.

✓ ***state1<12>: Bit SCA splitting.***

This bit makes it possible to split the SCA in two blocs of 256 analog memory cells in write & read modes (“0”: 512 cells; “1”: 2 x 256 cells).

✓ ***state1<13>: Bit 32 channels mode.***

This bit makes it possible to use only half of the channels (channels 1 to 32).

✓ ***state1<14>: Bit readout mode.***

This bit defines the readout of all channels (“1”), hit or selected channels (“0”).

✓ ***state1<15>: Bit FPN readout.***

It forces the readout of the FPN channels.

✓ ***state1<16>: Bit polarity.***

This bit controls the value of the DC voltage level (2 values) of the CSA, CR and Gain -2 according to the input signal polarity (table 11).

CSA	CR&SK	G2	Bit polarity	Detector signal
1.8V	2.2V	*0.7V*	*0*	*Neg. (CSA current out)*
2.8V	0.7V	*2.2V*	*1*	*Pos. (CSA current in)*

Table 11: CSA, CR, SK & Gain2 DC voltage versus bit polarity.

✓ ***state1<17:18>: Bit vicm0 to vicm1.***

These 2 bits change the input common mode voltage of the analog output buffer, according to the polarity of the signal and additional offset (table 12).

Vicm 1	Vicm 0	VICM value
0	0	*1.25V*
0	1	*1.35V*
1	0	*1.55V*
1	1	*1.65V*

Table 12: Definition of the Buffer vicm.

✓ ***state1<19:22>: Bit DAC0 to DAC sign.***

The first 3 bits define the value of the global threshold and the last bit (DAC sign) the polarity of the input signal (“0” for negative polarity).

✓ ***state1<23:24>: Bit trigger veto 0 to trigger veto 1.***

These 2 bits specify the use of veto on the trigger building (table 13).

veto 1	veto 0	veto
0	0	*none*
0	1	*4 µs*
1	0	*Hit register width*
1	1	*undefined*

Table 13: Definition of the trigger veto.

✓ ***state1<25>: Bit Synchro_discri.***

This bit permits (“1”) or not (“0”) to sample and synchronize the output discriminator on the rising edge of the SCAckwrite signal.

✓ ***state1<26>: Bit tot.***

This bit permits (“1”) or not (“0”) to have a trigger signal with the same width as the one of the discriminator output signal (Time Over Threshold).

✓ ***state1<27>: Bit Range_trigg_width.***

This bit defines the width range of the trigger signal (table 14).

Range_trigg_width	Width range (ns)
0	*100 ns*
1	*200 ns*

Table 14: Definition of the trigger width range.

✓ ***state1<28:29>: Bit lsb_trigg_width to msb_trigg_width.***

These 2 bits adjust the value of the trigger according to the process corners (table 15 & 16) and to the value of the Range_trigg_width value. They control also the value of unity multiplicity signal.

For Range_trigg_width = “0”.

Msb_trigg_width	Lsb_trigg_width	wp	tm	ws
0	0	*60.86 ns*	*93.88 ns*	*127.91 ns*
0	1	*49.8 ns*	*77.4 ns*	*106.25 ns*
1	0	*71.95 ns*	*110.36 ns*	*149.8 ns*
1	1	*82.86 ns*	*126.9 ns*	*171.6 ns*

Table 15: adjustment of the trigger width in the 100 ns range.

For Range_trigg_width = “1”.

Msb_trigg_width	Lsb_trigg_width	wp	tm	ws
0	0	*142 ns*	*218 ns*	*297 ns*
0	1	*110 ns*	*170 ns*	*232 ns*
1	0	*153 ns*	*235 ns*	*319 ns*
1	1	*194 ns*	*298 ns*	*404 ns*

Table 16: adjustment of the trigger width in the 200 ns range.

✓ ***state1<30:31>: Bit external 0 to external 1.***

These 2 bits specify the access point in the external mode (table 17).

external 1	external 0	Access point
0	0	*none*
0	1	*SK Filter input*
1	0	*Gain-2 input*
1	1	*CSA standby*

Table 17: Definition of the access point.

9.7.C Register 2

This 32-bit register is used to the test and to control the SCA reading (table 18). Only 24/32 bits are used in this register.

bit	name	action
0	**debug0**	These 3 bits select the internal signal to be view on scoop.
1	**debug1**	
2	**debug2**	
3	**read_from_0**	if 1, force to start the readout from column 0
4	**test_digout**	if 1, a test pattern is serialized to the output instead of the 9bit address of the last read column
5	**set_I0_when_rst**	Select the analog reset level during “reset operation”
6	**en_mker_rst**	if 1, a "digital" marker (near gnd or vdd levels) is multiplexed to the analog output during "reset operation"
7	**rst_lv_to 1**	set the level of the digital marker (when en_mker_rst=1)
8	**boost_pw**	If 1, the output current of the analog block Gain-2 is increased (+20%)
9	**out_resync**	If 1, the SC output data is resynchronized by a clock edge (selected by synchro_inv)
10	**synchro_inv**	select the edge for the synchronizing of the SC output data (0= rising, 1=falling)
11	**force_eout**	If 1, inhibit the 3rd state functionality of the SC output buffer.
12	**Cur_RA<0>**	These 2 bits manage the current of the SCA line buffers
13	**Cur_RA<1>**	
14	**Cur_BUF<0>**	These 2 bits manage the current of the SCA output buffers
15	**Cur_BUF<1>**	
16	**power_down_write**	if 1, put the write section in power down mode
17	**power_down_read**	if 1 put the read section in power down mode
18	**alternate_power**	if 1, set alternatively the read and write sections in power down mode.
19	**ShortReadSeq**	It control the length of the “reset level” in the SCA readout phase
20	**Dis_Multiplicity_Out**	If 1, disable the trigger output
21	**Autoreset Bank**	Select the reset mode of the SCA pointer.
22	**En_trigg_lvds**	if 1, enable the LVDS trigger signal on the output pads 85 & 86.
23		
24	**Input-dynamic-range**	This bit selects the input dynamic of the discriminator (5 or 17.5%).
25 to 31		

Table 18: Register 2.

- ✓ ***state2<0:2>: Bit Debug 0 to Debug 2.***

These 3 bits allows the user to view the outputs of the following signals on an oscilloscope: CSA, PZC filter, and Gain-2, or the 2 inputs of the discriminators for channel 1. It is also possible to view the trigger signal directly. Depending on the bits selected (table 19), one of the signals is multiplexed toward the ***Out_debug*** pin.

Debug2	Debug1	Debug0	Out_debug (canal1)
0	**0**	**0**	***Standby***
0	**0**	**1**	***CSA***
0	**1**	**0**	***CR***
0	**1**	**1**	***Gain-2***
1	**0**	**0**	***Positive input of the discriminator***
1	**0**	**1**	***negative input of the discriminator***
1	**1**	**0**	***trigger***
1	**1**	**1**	***none***

Table 19: Selection of the output in the “spy” mode.

Bit read_from_0; test_digout; set_I0_when_rst; en_mker_rst; rst_lv_to 1.

These 5 bits act directly on the readout of the SCA and are used essentially for testing the ASIC.

✓ ***state2<3>: read_from_0.***

In the normal mode, the readout starts from the column following the last written. Set this bit to "1", forces to start the readout from the physical column **0**.

✓ ***state2<4>: Test_digout.***

If this bit is set to"1", a test pattern ("101011001") is serialized to the output instead of the 9 bits address of the last read column.

✓ ***state2<5>: set_I0_when_rst.***

Specify the reset level of the analog output during the "reset operation". It must be set to "0".

✓ ***state2<6>: en_mker_rst.***

If "1", a "digital" marker (near gnd or vdd levels) is multiplexed to the analog output during the first of the "reset states".

✓ ***state2<7>: rst_lv_to 1.***

Set the level of the digital marker (when en_mker_rst="1"). "0" means level near gnd; "1" means level near Vdd.

✓ ***state2<8>: boost_pw.***

If 1, the output current of the GAIN-2 amplifier is increased by +20%. It can be used for very fast sampling frequencies and in case of chip fabricated in a "slow" corner process.

Bit out_resync, synchro_inv & force_eout.

These 3 bits change some configurations of the Slow Control.

✓ ***state2<9>: out_resync.***

If 1, the ***Sc_dout*** output data is resynchronized by a clock edge ***Sc_ck***, selected by ***synchro_inv***.

✓ ***state2<10>: synchro_inv.***

It selects the edge for the synchronizing of the ***Sc_dout*** output data. "0" select the rising edge, "1" the falling.

✓ ***state2<11>: force_eout.***

"1" inhibits the 3rd state functionality of the Slow Control output buffer.

✓ ***state2<12:13>: Bit CUR_RA <0:1>.***

These 2 bits control the bias current of the 68 SCA line readout buffers. This control is also managed by the bits ***power_down_read*** & ***alternate_power*** of register 2. Table 20 lists the different values of the readout buffer power current.

CUR_RA<1>	CUR_RA<0>	*power_down_read & alternate_power = "0"*	*power_down_read or alternate_power = "1"*
0	0	*352uA*	*292uA*
0	1	*450uA*	*352uA*
1	0	*637uA*	*450uA*
1	1	*1150uA*	*637uA*

Table 20: Control of the SCA line buffer current.

The nominal configuration is: « **10** ».

✓ ***state2<14:15>: Bit CUR_BUF <0:1>.***

These 2 bits control the bias current of the group multiplexor buffer of the 2 groups (one buffer for 34 lines) and of the final multiplexor buffer. These buffers provide an optimal settling time of the SCA analog data sending it through the differential output buffer. Table 21 shows different values of the power current for these 3 buffers.

CUR_BUF<1>	CUR_BUF<0>	I power
0	0	*1.503 mA*
0	1	*1.914 mA*
1	0	*2.700 mA*
1	1	*4.870 mA*

Table 21: Control of the SCA multiplexor buffers current.

The nominal configuration is: « **10** ».

✓ ***state2<16:18>: Bit power_down_write, power_down_read & alternate_power.***

These bits manage the power consumption. When the chip is in the write mode, the reading part is not used and therefore the SCA line buffer can be put in a standby mode. In the read mode, as the analog data is stored in the SCA, the writing part of the analog channel (pole-zero cancellation stage, Sallen&Key filter, and Gain-2) is put also in a standby mode. This functional mode is activated by the bit ***alternate_power***. It is also possible to force independently the writing and the reading parts in a standby mode by the bits ***power_down_write*** and ***power_down_read***.

✓ ***state2<19>: Bit ShortReadSeq.***

This bit controls the length of the “reset level” data which is initially sent before the analog data of each SCA column in the SCA readout phase.
For “0”, we will have: 2 bits of reset level + 2 bits of indeterminate level.
For “1”, 1 bit of reset level + 1 bit of indeterminate level.

✓ ***state2<20>: Bit Dis_Multiplicity_Out.***

This bit enables (“0”) or disables (“1”) the output of the trigger signal.

✓ ***state2<21>: Bit Autoreset Bank.***

This bit controls the reset of the SCA pointer. For “0”, the reset is done on the write signal with a width equal to the SCAwrite clock. For “1”, the reset is done automatically on the rising edge of the write signal.

✓ ***state2<22>: Bit En_trigg_lvds.***

This bit permits to disable (“0”) or enable (“1”) the output of the trigger signal in LVDS level on the pads 85 & 86.

✓ ***state2<24>: Bit input-dynamic-range.***

This bit permits to select the value of input dynamic range of the discriminator between two values: 5 or 17.5 % of the channel input dynamic range.

State2<24>	Input dynamic range
0	*17.5 %*
1	*5 %*

Table 22: Definition of the input dynamic range of the discriminator.

9.7.D Register 3

This 34 bits register is located at address number 3. It is used to select the channel for the test (table 23). The channel number goes from 1 to 32, and 1 to 2 for the FPN channels.

bit	name	action
0	**select_c32**	Selection of the channel 32 for the test
1	**select_c31**	Selection of the channel 31 for the test
2	**select_c30**	Selection of the channel 30 for the test
3	**select_c29**	Selection of the channel 29 for the test
4	**select_c28**	Selection of the channel 28 for the test
5	**select_c27**	Selection of the channel 27 for the test
6	**select_c26**	Selection of the channel 26 for the test
7	**select_c25**	Selection of the channel 25 for the test
8	**select_c24**	Selection of the channel 24 for the test
9	**select_c23**	Selection of the channel 23 for the test
10	**select_c22**	Selection of the channel 22 for the test
11	**select_cfpn2**	Selection of the channel cfpn2 for the test
12	**select_c21**	Selection of the channel 21 for the test
13	**select_c20**	Selection of the channel 20 for the test
14	**select_c19**	Selection of the channel 19 for the test
15	**select_c18**	Selection of the channel 18 for the test
16	**select_c17**	Selection of the channel 17 for the test
17	**select_c16**	Selection of the channel 16 for the test
18	**select_c15**	Selection of the channel 15 for the test
19	**select_c14**	Selection of the channel 14 for the test
20	**select_c13**	Selection of the channel 13 for the test
21	**select_c12**	Selection of the channel 12 for the test
22	**select_cfpn1**	Selection of the channel cfpn1 for the test
23	**select_c11**	Selection of the channel 11 for the test
24	**select_c10**	Selection of the channel 10 for the test
25	**select_c9**	Selection of the channel 9 for the test
26	**select_c8**	Selection of the channel 8 for the test
27	**select_c7**	Selection of the channel 7 for the test
28	**select_c6**	Selection of the channel 6 for the test
29	**select_c5**	Selection of the channel 5 for the test
30	**select_c4**	Selection of the channel 4 for the test
31	**select_c3**	Selection of the channel 3 for the test
32	**select_c2**	Selection of the channel 2 for the test
33	**select_c1**	Selection of the channel 1 for the test

Table 23: Description of the register 3.

9.7.E Register 4

This 34 bits register is located at address number 4. It is used to select the channel for the test (table 24). The channel number goes from 33 to 64, and 3 to 4 for the FPN channels.

bit	name	action
0	**select_c33**	Selection of the channel 33 for the test
1	**select_c34**	Selection of the channel 34 for the test
2	**select_c35**	Selection of the channel 35 for the test
3	**select_c36**	Selection of the channel 36 for the test
4	**select_c37**	Selection of the channel 37 for the test
5	**select_c38**	Selection of the channel 38 for the test
6	**select_c39**	Selection of the channel 39 for the test
7	**select_c40**	Selection of the channel 40 for the test
8	**select_c41**	Selection of the channel 41 for the test
9	**select_c42**	Selection of the channel 42 for the test
10	**select_c43**	Selection of the channel 43 for the test
11	**select_cfpn3**	Selection of the channel cfpn3 for the test
12	**select_c44**	Selection of the channel 44 for the test
13	**select_c45**	Selection of the channel 45 for the test
14	**select_c46**	Selection of the channel 46 for the test
15	**select_c47**	Selection of the channel 47 for the test
16	**select_c48**	Selection of the channel 48 for the test
17	**select_c49**	Selection of the channel 49 for the test
18	**select_c50**	Selection of the channel 50 for the test
19	**select_c51**	Selection of the channel 51 for the test
20	**select_c52**	Selection of the channel 52 for the test
21	**select_c53**	Selection of the channel 53 for the test
22	**select_cfpn4**	Selection of the channel cfpn4 for the test
23	**select_c54**	Selection of the channel 54 for the test
24	**select_c55**	Selection of the channel 55 for the test
25	**select_c56**	Selection of the channel 56 for the test
26	**select_c57**	Selection of the channel 57 for the test
27	**select_c58**	Selection of the channel 58 for the test
28	**select_c59**	Selection of the channel 59 for the test
29	**select_c60**	Selection of the channel 60 for the test
30	**select_c61**	Selection of the channel 61 for the test
31	**select_c62**	Selection of the channel 62 for the test
32	**select_c63**	Selection of the channel 63 for the test
33	**select_c64**	Selection of the channel 64 for the test

Table 24: Description of the register 4.

9.7.F Register 5

This 16 bits register is located at address number 5. It contains the version number of the chip. The version number is: 0x0202 (0x0201 in prototype version).

9.7.G Register 6

This 64 bits register defines the gain of the 32 first channels. Each channel needs a 2 bit register to select its CSA charge capacitor among 4. The mapping is given in the table 25.
At the channel level, the gain is defined as follows:

MSB	LSB	*Charge range*
0	**0**	***120 fC***
0	**1**	***240 fC***
1	**0**	***1 pC***
1	**1**	***10 pC***

bit	name	action	bit	name	action
0	**Lsb Gain c32**		32	**Lsb Gain c16**	
1	**Msb Gain c32**	Gain selection channel 32	33	**Msb Gain c16**	Gain selection channel 16
2	**Lsb Gain c**31		34	**Lsb Gain c**15	
3	**Msb Gain c**31	Gain selection channel 31	35	**Msb Gain c**15	Gain selection channel 15
4	**Lsb Gain c30**		36	**Lsb Gain c14**	
5	**Msb Gain c30**	Gain selection channel 30	37	**Msb Gain c14**	Gain selection channel 14
6	**Lsb Gain c29**		38	**Lsb Gain c13**	
7	**Msb Gain c29**	Gain selection channel 29	39	**Msb Gain c13**	Gain selection channel 13
8	**Lsb Gain c28**		40	**Lsb Gain c12**	
9	**Msb Gain c28**	Gain selection channel 28	41	**Msb Gain c12**	Gain selection channel 12
10	**Lsb Gain c27**		42	**Lsb Gain c11**	
11	**Msb Gain c27**	Gain selection channel 27	43	**Msb Gain c11**	Gain selection channel 11
12	**Lsb Gain c26**		44	**Lsb Gain c10**	
13	**Msb Gain c26**	Gain selection channel 26	45	**Msb Gain c10**	Gain selection channel 10
14	**Lsb Gain c25**		46	**Lsb Gain c09**	
15	**Msb Gain c25**	Gain selection channel 25	47	**Msb Gain c09**	Gain selection channel 9
16	**Lsb Gain c24**		48	**Lsb Gain c08**	
17	**Msb Gain c24**	Gain selection channel 24	49	**Msb Gain c08**	Gain selection channel 8
18	**Lsb Gain c23**		50	**Lsb Gain c07**	
19	**Msb Gain c23**	Gain selection channel 23	51	**Msb Gain c07**	Gain selection channel 7
20	**Lsb Gain c22**		52	**Lsb Gain c06**	
21	**Msb Gain c22**	Gain selection channel 22	53	**Msb Gain c06**	Gain selection channel 6
22	**Lsb Gain c21**		54	**Lsb Gain c05**	
23	**Msb Gain c21**	Gain selection channel 21	55	**Msb Gain c05**	Gain selection channel 5
24	**Lsb Gain c20**		56	**Lsb Gain c04**	
25	**Msb Gain c20**	Gain selection channel 20	57	**Msb Gain c04**	Gain selection channel 4
26	**Lsb Gain c19**		58	**Lsb Gain c03**	
27	**Msb Gain c19**	Gain selection channel 19	59	**Msb Gain c03**	Gain selection channel 3
28	**Lsb Gain c18**		60	**Lsb Gain c02**	
29	**Msb Gain c18**	Gain selection channel 18	61	**Msb Gain c02**	Gain selection channel 2
30	**Lsb Gain c17**		62	**Lsb Gain c01**	
31	**Msb Gain c17**	Gain selection channel 17	63	**Msb Gain c01**	Gain selection channel 1

Table 25: Description of the register 6.

9.7.H Register 7

This 64 bits register defines the gain of the last 32 channels. Each channel needs a 2 bit register to select its CSA charge capacitor among 4. The mapping is given in the table 26.

bit	name	action	bit	name	action
0	**Lsb Gain c33**		32	**Lsb Gain c49**	
1	**Msb Gain c33**	Gain selection channel 33	33	**Msb Gain c49**	Gain selection channel 49
2	**Lsb Gain c**34		34	**Lsb Gain c**50	
3	**Msb Gain c**34	Gain selection channel 34	35	**Msb Gain c**50	Gain selection channel 50
4	**Lsb Gain c35**		36	**Lsb Gain c51**	
5	**Msb Gain c35**	Gain selection channel 35	37	**Msb Gain c51**	Gain selection channel 51
6	**Lsb Gain c36**		38	**Lsb Gain c52**	
7	**Msb Gain c36**	Gain selection channel 36	39	**Msb Gain c52**	Gain selection channel 52
8	**Lsb Gain c37**		40	**Lsb Gain c53**	
9	**Msb Gain c37**	Gain selection channel 37	41	**Msb Gain c53**	Gain selection channel 53
10	**Lsb Gain c38**		42	**Lsb Gain c54**	
11	**Msb Gain c38**	Gain selection channel 38	43	**Msb Gain c54**	Gain selection channel 54
12	**Lsb Gain c39**		44	**Lsb Gain c55**	
13	**Msb Gain c39**	Gain selection channel 39	45	**Msb Gain c55**	Gain selection channel 55
14	**Lsb Gain c40**		46	**Lsb Gain c56**	
15	**Msb Gain c40**	Gain selection channel 40	47	**Msb Gain c56**	Gain selection channel 56
16	**Lsb Gain c41**		48	**Lsb Gain c57**	
17	**Msb Gain c41**	Gain selection channel 41	49	**Msb Gain c57**	Gain selection channel 57
18	**Lsb Gain c42**		50	**Lsb Gain c58**	
19	**Msb Gain c42**	Gain selection channel 42	51	**Msb Gain c58**	Gain selection channel 58
20	**Lsb Gain c43**		52	**Lsb Gain c59**	
21	**Msb Gain c43**	Gain selection channel 43	53	**Msb Gain c59**	Gain selection channel 59
22	**Lsb Gain c44**		54	**Lsb Gain c60**	
23	**Msb Gain c44**	Gain selection channel 44	55	**Msb Gain c60**	Gain selection channel 60
24	**Lsb Gain c45**		56	**Lsb Gain c61**	
25	**Msb Gain c45**	Gain selection channel 45	57	**Msb Gain c61**	Gain selection channel 61
26	**Lsb Gain c46**		58	**Lsb Gain c62**	
27	**Msb Gain c46**	Gain selection channel 46	59	**Msb Gain c62**	Gain selection channel 62
28	**Lsb Gain c47**		60	**Lsb Gain c63**	
29	**Msb Gain c47**	Gain selection channel 47	61	**Msb Gain c63**	Gain selection channel 63
30	**Lsb Gain c48**		62	**Lsb Gain c64**	
31	**Msb Gain c48**	Gain selection channel 48	63	**Msb Gain c64**	Gain selection channel 64

Table 26: Description of the register 7.

9.7.I Register 8

This 128 bits register defines the value of the individual threshold for channels 1 to 32. Each channel needs a 4-bit register to control its DAC. The mapping is given in the table 27.

bit	name	action
0	**Lsb threshold c32**	
1	**Bit 1 threshold c32**	
2	**Bit 2 threshold c32**	
3	**Msb threshold c32**	Threshold channel 32
4	**Lsb threshold c31**	
5	**Bit 1 threshold c31**	
6	**Bit 2 threshold c31**	
7	**Msb threshold c31**	Threshold channel 31
8	**Lsb threshold c30**	
9	**Bit 1 threshold c30**	
10	**Bit 2 threshold c30**	
11	**Msb threshold c30**	Threshold channel 30
12 to 63	***C 29 to c17***	*Threshold channel 29 to 17*
64	**Lsb threshold c16**	
65	**Bit 1 threshold c16**	
66	**Bit 2 threshold c16**	
67	**Msb threshold c16**	Threshold channel 16
68	**Lsb threshold c15**	
69	**Bit 1 threshold c15**	
70	**Bit 2 threshold c15**	
71	**Msb threshold c15**	Threshold channel 15
72 to 115	***C 14 to c4***	*Threshold channel 14 to 4*
116	**Lsb threshold c3**	
117	**Bit 1 threshold c3**	
118	**Bit 2 threshold c3**	
119	**Msb threshold c3**	Threshold channel 3
120	**Lsb threshold c2**	
121	**Bit 1 threshold c2**	
122	**Bit 2 threshold c2**	
123	**Msb threshold c2**	Threshold channel 2
124	**Lsb threshold c1**	
125	**Bit 1 threshold c1**	
126	**Bit 2 threshold c1**	
127	**Msb threshold c1**	Threshold channel 1

Table 27: Description of the register 8.

9.7.J Register 9

This 128 bits register defines the value of the individual threshold for channels 33 to 64. Each channel needs a 4 bits register to control its DAC. The mapping is given in the table 28.

bit	name	action
0	**Lsb threshold c33**	
1	**Bit 1 threshold c33**	
2	**Bit 2 threshold c33**	
3	**Msb threshold c33**	Threshold channel 33
4	**Lsb threshold c34**	
5	**Bit 1 threshold c34**	
6	**Bit 2 threshold c34**	
7	**Msb threshold c34**	Threshold channel 34
8	**Lsb threshold c35**	
9	**Bit 1 threshold c35**	
10	**Bit 2 threshold c35**	
11	**Msb threshold c35**	Threshold channel 35
12 to 63	***c36 to c48***	*Threshold channel 36 to 48*
64	**Lsb threshold c49**	
65	**Bit 1 threshold c49**	
66	**Bit 2 threshold c49**	
67	**Msb threshold c49**	Threshold channel 49
68	**Lsb threshold c50**	
69	**Bit 1 threshold c50**	
70	**Bit 2 threshold c50**	
71	**Msb threshold c50**	Threshold channel 50
72 to 115	***c51 to c61***	*Threshold channel 51 to 61*
116	**Lsb threshold c62**	
117	**Bit 1 threshold c62**	
118	**Bit 2 threshold c62**	
119	**Msb threshold c62**	Threshold channel 62
120	**Lsb threshold c63**	
121	**Bit 1 threshold c63**	
122	**Bit 2 threshold c63**	
123	**Msb threshold c63**	Threshold channel 63
124	**Lsb threshold c64**	
125	**Bit 1 threshold c64**	
126	**Bit 2 threshold c64**	
127	**Msb threshold c64**	Threshold channel 64

Table 28: Description of the register 9.

9.7.K Register 10

This 64 bits register permits to inhibit a specific channel to the trigger building or to the trigger data (trigger building & hit register). The mapping for channels 1 to 32 is given in the table 29.

bit	name	action	bit	name	action
0	**Lsb Inhi c32**	Inhibit channel 32	32	**Lsb Inhi c16**	Inhibit channel 16
1	**Msb Inhi c32**	Inhibit trigger channel 32	33	**Msb Inhi c16**	Inhibit trigger channel 16
2	**Lsb Inhi c**31	Inhibit channel 31	34	**Lsb Inhi c**15	Inhibit channel 15
3	**Msb Inhi c**31	Inhibit trigger channel 31	35	**Msb Inhi c**15	Inhibit trigger channel 15
4	**Lsb Inhi c30**	Inhibit channel 30	36	**Lsb Inhi c14**	Inhibit channel 14
5	**Msb Inhi c30**	Inhibit trigger channel 30	37	**Msb Inhi c14**	Inhibit trigger channel 14
6	**Lsb Inhi c29**	Inhibit channel 29	38	**Lsb Inhi c13**	Inhibit channel 13
7	**Msb Inhi c29**	Inhibit trigger channel 29	39	**Msb Inhi c13**	Inhibit trigger channel 13
8	**Lsb Inhi c28**	Inhibit channel 28	40	**Lsb Inhi c12**	Inhibit channel 12
9	**Msb Inhi c28**	Inhibit trigger channel 28	41	**Msb Inhi c12**	Inhibit trigger channel 12
10	**Lsb Inhi c27**	Inhibit channel 27	42	**Lsb Inhi c11**	Inhibit channel 11
11	**Msb Inhi c27**	Inhibit trigger channel 27	43	**Msb Inhi c11**	Inhibit trigger channel 11
12	**Lsb Inhi c26**	Inhibit channel 26	44	**Lsb Inhi c10**	Inhibit channel 10
13	**Msb Inhi c26**	Inhibit trigger channel 26	45	**Msb Inhi c10**	Inhibit trigger channel 10
14	**Lsb Inhi c25**	Inhibit channel 25	46	**Lsb Inhi c09**	Inhibit channel 9
15	**Msb Inhi c25**	Inhibit trigger channel 25	47	**Msb Inhi c09**	Inhibit trigger channel 9
16	**Lsb Inhi c24**	Inhibit channel 24	48	**Lsb Inhi c08**	Inhibit channel 8
17	**Msb Inhi c24**	Inhibit trigger channel 24	49	**Msb Inhi c08**	Inhibit trigger channel 8
18	**Lsb Inhi c23**	Inhibit channel 23	50	**Lsb Inhi c07**	Inhibit channel 7
19	**Msb Inhi c23**	Inhibit trigger channel 23	51	**Msb Inhi c07**	Inhibit trigger channel 7
20	**Lsb Inhi c22**	Inhibit channel 22	52	**Lsb Inhi c06**	Inhibit channel 6
21	**Msb Inhi c22**	Inhibit trigger channel 22	53	**Msb Inhi c06**	Inhibit trigger channel 6
22	**Lsb Inhi c21**	Inhibit channel 21	54	**Lsb Inhi c05**	Inhibit channel 5
23	**Msb Inhi c21**	Inhibit trigger channel 21	55	**Msb Inhi c05**	Inhibit trigger channel 5
24	**Lsb Inhi c20**	Inhibit channel 20	56	**Lsb Inhi c04**	Inhibit channel 4
25	**Msb Inhi c20**	Inhibit trigger channel 20	57	**Msb Inhi c04**	Inhibit trigger channel 4
26	**Lsb Inhi c19**	Inhibit channel 19	58	**Lsb Inhi c03**	Inhibit channel 3
27	**Msb Inhi c19**	Inhibit trigger channel 19	59	**Msb Inhi c03**	Inhibit trigger channel 3
28	**Lsb Inhi c18**	Inhibit channel 18	60	**Lsb Inhi c02**	Inhibit channel 2
29	**Msb Inhi c18**	Inhibit trigger channel 18	61	**Msb Inhi c02**	Inhibit trigger channel 2
30	**Lsb Inhi c17**	Inhibit channel 17	62	**Lsb Inhi c01**	Inhibit channel 1
31	**Msb Inhi c17**	Inhibit trigger channel 17	63	**Msb Inhi c01**	Inhibit trigger channel 1

Table 29: Description of the register 10.

9.7.L Register 11

This 64 bits register permits to inhibit a specific channel to the trigger building or to the trigger data (trigger building & hit register). The mapping for channels 33 to 64 is given in the table 30.

bit	name	action	bit	name	action
0	**Lsb Inhi c33**	Inhibit channel 33	32	**Lsb Inhi c49**	Inhibit channel 49
1	**Msb Inhi c33**	Inhibit trigger channel 33	33	**Msb Inhi c49**	Inhibit trigger channel 49
2	**Lsb Inhi c**34	Inhibit channel 34	34	**Lsb Inhi c**50	Inhibit channel 50
3	**Msb Inhi c**34	Inhibit trigger channel 34	35	**Msb Inhi c**50	Inhibit trigger channel 50
4	**Lsb Inhi c35**	Inhibit channel 35	36	**Lsb Inhi c51**	Inhibit channel 51
5	**Msb Inhi c35**	Inhibit trigger channel 35	37	**Msb Inhi c51**	Inhibit trigger channel 51
6	**Lsb Inhi c36**	Inhibit channel 36	38	**Lsb Inhi c52**	Inhibit channel 52
7	**Msb Inhi c36**	Inhibit trigger channel 36	39	**Msb Inhi c52**	Inhibit trigger channel 52
8	**Lsb Inhi c37**	Inhibit channel 37	40	**Lsb Inhi c53**	Inhibit channel 53
9	**Msb Inhi c37**	Inhibit trigger channel 37	41	**Msb Inhi c53**	Inhibit trigger channel 53
10	**Lsb Inhi c38**	Inhibit channel 38	42	**Lsb Inhi c54**	Inhibit channel 54
11	**Msb Inhi c38**	Inhibit trigger channel 38	43	**Msb Inhi c54**	Inhibit trigger channel 54
12	**Lsb Inhi c39**	Inhibit channel 39	44	**Lsb Inhi c55**	Inhibit channel 55
13	**Msb Inhi c39**	Inhibit trigger channel 39	45	**Msb Inhi c55**	Inhibit trigger channel 55
14	**Lsb Inhi c40**	Inhibit channel 40	46	**Lsb Inhi c56**	Inhibit channel 56
15	**Msb Inhi c40**	Inhibit trigger channel 40	47	**Msb Inhi c56**	Inhibit trigger channel 56
16	**Lsb Inhi c41**	Inhibit channel 41	48	**Lsb Inhi c57**	Inhibit channel 57
17	**Msb Inhi c41**	Inhibit trigger channel 41	49	**Msb Inhi c57**	Inhibit trigger channel 57
18	**Lsb Inhi c42**	Inhibit channel 42	50	**Lsb Inhi c58**	Inhibit channel 58
19	**Msb Inhi c42**	Inhibit trigger channel 42	51	**Msb Inhi c58**	Inhibit trigger channel 58
20	**Lsb Inhi c43**	Inhibit channel 43	52	**Lsb Inhi c59**	Inhibit channel 59
21	**Msb Inhi c43**	Inhibit trigger channel 43	53	**Msb Inhi c59**	Inhibit trigger channel 59
22	**Lsb Inhi c44**	Inhibit channel 44	54	**Lsb Inhi c60**	Inhibit channel 60
23	**Msb Inhi c44**	Inhibit trigger channel 44	55	**Msb Inhi c60**	Inhibit trigger channel 60
24	**Lsb Inhi c45**	Inhibit channel 45	56	**Lsb Inhi c61**	Inhibit channel 61
25	**Msb Inhi c45**	Inhibit trigger channel 45	57	**Msb Inhi c61**	Inhibit trigger channel 61
26	**Lsb Inhi c46**	Inhibit channel 46	58	**Lsb Inhi c62**	Inhibit channel 62
27	**Msb Inhi c46**	Inhibit trigger channel 46	59	**Msb Inhi c62**	Inhibit trigger channel 62
28	**Lsb Inhi c47**	Inhibit channel 47	60	**Lsb Inhi c63**	Inhibit channel 63
29	**Msb Inhi c47**	Inhibit trigger channel 47	61	**Msb Inhi c63**	Inhibit trigger channel 63
30	**Lsb Inhi c48**	Inhibit channel 48	62	**Lsb Inhi c64**	Inhibit channel 64
31	**Msb Inhi c48**	Inhibit trigger channel 48	63	**Msb Inhi c64**	Inhibit trigger channel 64

Table 30: Description of the register 11.

9.7.M Register 12

This 16-bit register permits to reduce the number of SCA memory cell during the readout phase by adding an offset (9 bits) on the readout pointer address. Only the first 9 bits are used.

10. Power supply connections

A significant number of pins of the AGET chip (27 Vdd; 30 Gnd) are dedicated to power supplies. The analog channels of AGET are split into 2 groups of 34, for matching a square package. The height of these 2 groups (8 mm) and the sensitivity of each block (CSA, CR, SK, G-2, Discriminator & DAC threshold) imply to supply these blocks independently and homogeneously (Pins in top & bottom). This is also true for the SCA powering. The **Fig. 30** shows the internal architecture of the chip by indicating the placement and the name of various building blocks.

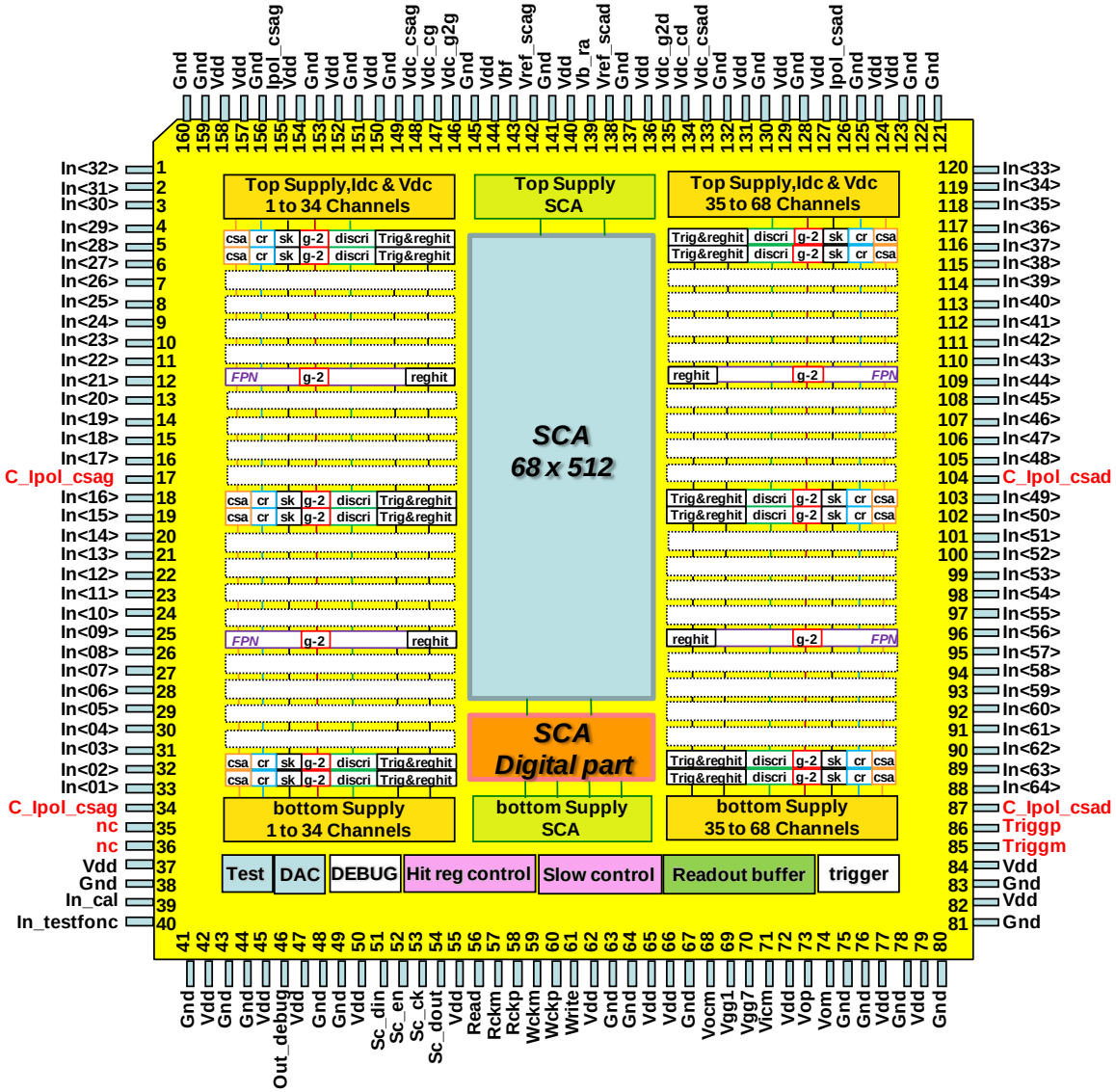


Fig. 30: Internal architecture of the AGET chip.

All the Vdd (Gnd) pads can be connected to the same PCB Vdd (Gnd) plan. A decoupling ceramic capacitor of 100 nF must be placed as close as possible to Vdd pins. An additional capacitor of 10 µF must be added for pads: 37, 84, 123,124, 157 & 158.

10.1 Cavity connection

The substrat (P type) of the chip must be connected to the ground. This is done by connecting the bottom of the package cavity with 4 pins in each corner (**Fig. 31**).

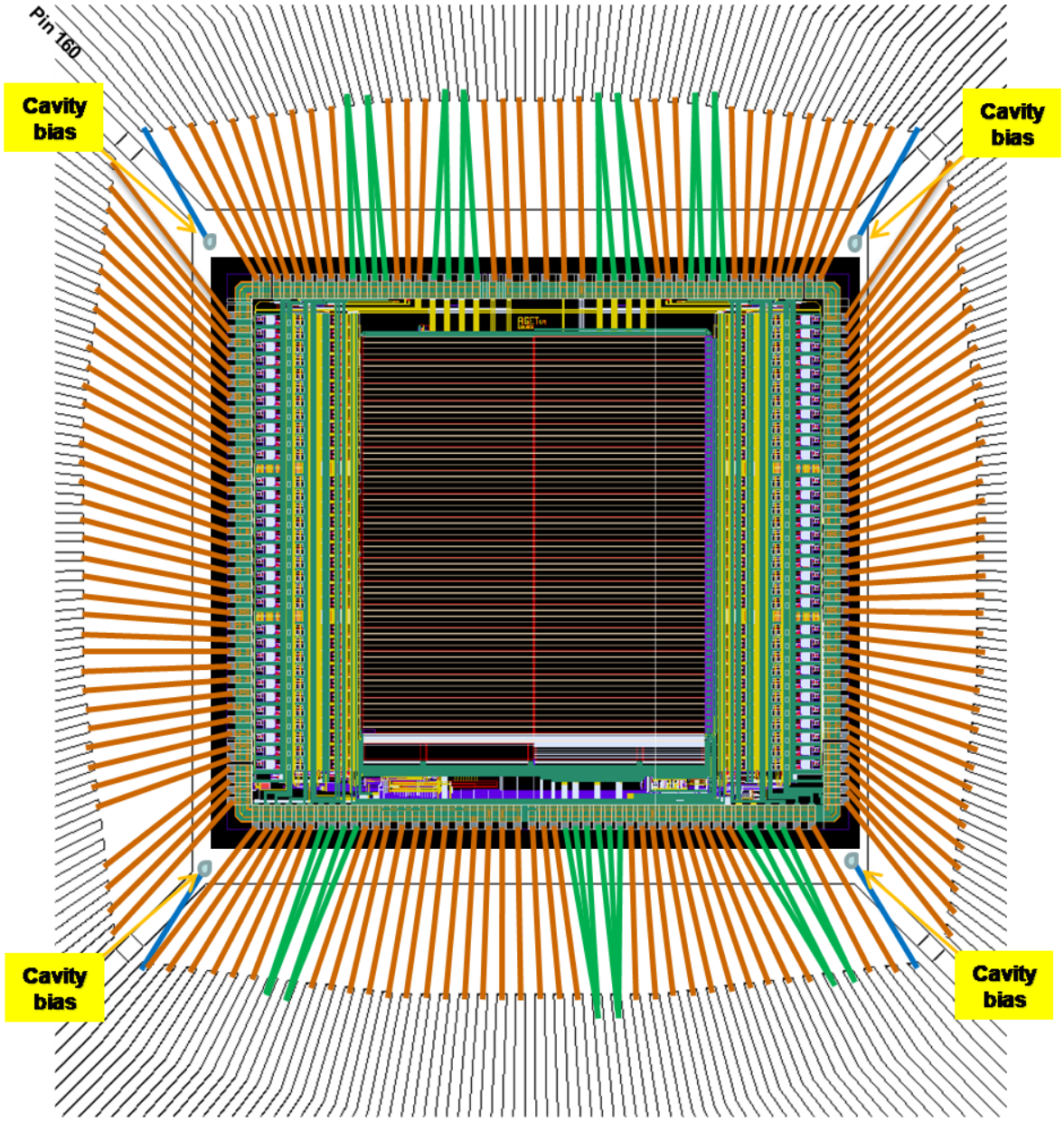


Fig. 31: Bonding diagram of the AGET chip.

N° pin	Name	Current value	Description
41	Gnd_Substrat	*0 A*	*Cavity; Protection diode [37 to 86]; SCA digital part guard ring.*
80	Gnd_Substrat	*0 A*	*Cavity*
121	Gnd_Substrat	*0 A*	*Cavity*
160	Gnd_Substrat	*0 A*	*Cavity*

Table 31: Pins for the cavity connection.

Pin 41 is used also for the input protection diodes of pin 37 to 86 and guard ring of the digital part of the SCA.

10.2 Protection diode bias

All the pins of the chip are protected by internal diodes. The power supplies of these diodes are carried out by independent pins. The pin n° 41 & 55 are used also to supply the SCA digital guard ring.

N° pin	Name	Current value	Description
41	Gnd_prob	*0 A*	*Gnd for: Cavity; Protection diodes [37 to 86]; SCA digital part guard ring.*
55	Vdd_prob	*0 A*	*Vdd for: Protection diodes [37 to 86]; SCA digital part guard ring.*
122	Gnd_proind	*0 A*	*Gnd for protection diodes [87 to 120]*
123	Vdd_proind	*0 A*	*Vnd for protection diodes [87 to 120]*
140	Vdd_proh	*0 A*	*Vdd for protection diodes [124 to 157]*
141	Gnd_proh	*0 A*	*Gnd for protection diodes [124 to 157]*
158	Vdd_proing	*0 A*	*Vdd for protection diodes [1 to 34]*
159	Gnd_proing	*0 A*	*Gnd for protection diodes [1to 34]*

Table 32: Pins for the protection diodes bias.

10.3 Front-end bias

The front-end is made of 5 blocks: CSA, PZC, SK, Gain-2 & Trigger (Gain & Discriminator). Each of them uses dedicated pins for power supplies, excepted for the Trigger block. The analog & digital aspect of this functionality and the lack of free pins forced us to use the bias of other blocks.

10.3.A CSA bias

The DC power consumption current depends on 2 parameters:

- The value of CSA nominal bias current set externally on the host card (ASAD card) by resistors connected to the pins: Ipol_csad (pin n° 126) & Ipol_csag (pin n° 155),
- The state1<0> of register 1. If “0”, the CSA bias current is nominal. If “1”, the nominal current is doubled.

N° pin	Name	Idc (mA)	Description
37	Vdd_csag	*3(5) + Ipol_csagx[0.5 +16x(1+”state<0>reg1”)]*	*Vdd & Gnd for:* • *CSA channel 1 to 32,* • *Threshold DAC.*
38	Gnd_csag	*3(5) + Ipol_csagx[0.5 +16x(1+”state<0>reg1”)]*	
156	Gnd_csag	*3(5) + Ipol_csagx[0.5 +16x(1+”state<0>reg1”)]*	
157	Vdd_csag	*3(5) + Ipol_csagx[0.5 +16x(1+”state<0>reg1”)]*	
83	Gnd_csad	*3(5) + Ipol_csadx[0.5 +16x(1+”state<0>reg1”)]*	*Vdd & Gnd for:* • *CSA channel 33 to 64,* • *Threshold DAC.*
84	Vdd_csad	*3(5) + Ipol_csadx[0.5 +16x(1+”state<0>reg1”)]*	
124	Vdd_csad	*3(5) + Ipol_csadx[0.5 +16x(1+”state<0>reg1”)]*	
125	Gnd_csad	*3(5) + Ipol_csadx[0.5 +16x(1+”state<0>reg1”)]*	

Table 33: Pins for the CSA bias.

The CSA bias is used also to supply the threshold part of the discriminator [global DAC + Channel DAC]. The bias current will depend on the threshold value choose.
In the case where:

- Ipol_csa = 400 µA & state<0> = “0”, the current per pin is 9.6 mA to 11.6 mA.
- Ipol_csa = 400 µA & state<0> = “1”, the current per pin is 16 mA to 18 mA.

10.3.B Pole-Zero-Cancellation stage bias

N° pin	Name	Idc (mA)	Description
42	Vdd_crg	*5.3*	*Vdd & Gnd for PZC channel 1 to 32.*
43	Gnd_crg	*5.3*	
153	Gnd_crg	*5.3*	
154	Vdd_crg	*5.3*	
81	Gnd_crd	*5.3*	*Vdd & Gnd for PZC channel 33 to 64.*
82	Vdd_crd	*5.3*	
127	Vdd_crd	*5.3*	
128	Gnd_crd	*5.3*	

Table 34: Pins for the PZC bias.

10.3.C SK filter stage bias

N° pin	Name	Idc (mA)	Description
44	Gnd_skg	*1.76*	*Vdd & Gnd for SK filter channel 1 to 32.*
45	Vdd_skg	*1.76*	
151	Gnd_skg	*1.76*	
152	Vdd_skg	*1.76*	
78	Gnd_skd	*1.76*	*Vdd & Gnd for SK filter channel 33 to 64.*
79	Vdd_skd	*1.76*	
129	Vdd_skd	*1.76*	
130	Gnd_skd	*1.76*	

Table 35: Pins for the SK filter bias.

10.3.D Inverting Gain-2 stage bias

N° pin	Name	Idc (mA)	Description
47	Vdd_g2g	*12.27*	*Vdd & Gnd for:* • *Gain-2 channel 1 to 32 & 2FPN,* • *Threshold gain channel 1 to 32,* • *Discriminator channel 1 to 32.*
48	Gnd_g2g	*12.27*	
149	Gnd_g2g	*12.27*	
150	Vdd_g2g	*12.27*	
76	Gnd_g2d	*12.27*	*Vdd & Gnd for:* • *Gain-2 channel 33 to 64 & 2FPN,* • *Threshold gain channel 33 to 64,* • *Discriminator channel 33 to 64.*
77	Vdd_g2d	*12.27*	
131	Vdd_g2d	*12.27*	
132	Gnd_g2d	*12.27*	

Table 36: Pins for the Gain-2 bias.

10.4 SCA power supplies

The SCA is divided into 4 parts: The matrix (512 x 68 analog cells), the input stage “return buffers” (1 per line), the SCA read amplifier (1 per line) and the digital part (clock, address …).

10.4.A Analog memory cell matrix

The supply of the matrix is made by a metal grid on its entire surface. This grid is connected to the power bus supply of the return and output buffers. The DC power consumption of this part is zero.

10.4.B "Return buffer" amplifiers

This stage buffers the Vreturn voltage (Vref_scag [pin n° 142]) to provide it as a reference to the memory cells.

N° pin	Name	Idc (mA)	Description
49	Gnd	3.4	***Vdd & Gnd for:*** • *"return buffer",* • *Matrix.*
50	Vdd	3.4	
144	Vdd	3.4	
145	Gnd	3.4	

Table 37: Pins for the "return buffer" amplifiers.

10.4.C SCA read amplifiers

This amplifier is used to read back the analog data stored in the memory cells. It is active only during the read phase. Its power consumption value is adjustable by slow control (bit CUR_RA <1:0> state<13:12> of reg. 2).

N° pin	Name	Idc (mA)	Description
66	Vdd	21.6	***Vdd & Gnd for:*** • *SCA read amplifier,* • *Matrix.* **For state2<13:12> = <1:0>**
67	Gnd	21.6	
136	Vdd	21.6	
137	Gnd	21.6	

Table 38: Pins for the SCA read amplifiers.

10.4.D SCA digital part

This part generates and distributes the signals required for the writing and reading operations in the SCA. Its power consumption is zero, excepted for the LVDS input buffers. The pins 64 & 65 are used also to supply the trigger generation, the slow control and hit channel register access.

N° pin	Name	Idc (mA)	Description
62	Vdd	0.509	***Vdd & Gnd for:*** • *LVDS receivers,* • *SCA write clock block.*
63	Gnd	0.509	
64	Gnd	10.33	***Vdd & Gnd for:*** • *SCA logic part,* • *Slow & hit register control,* • *Trigger.*
65	Vdd	10.33	

Table 39: Pins for the SCA digital part.

10.5 Readout output buffers

This section of the chip includes the analog output multiplexer, several intermediate buffers and the differential output buffer. The bias current of the intermediate buffers is controlled by the state<15:14> of register 2, the output buffer by two external pins: Vgg1 (pin n° 69) & Vgg7 (pin n°70).

N° pin	Name	Idc (mA)	Description
72	Vdd_out	17.3	***Vdd & Gnd for the readout output buffers***
75	Gnd	17.3	

Table 40: Pins for the readout output buffers.

10.6 Channel power consumption

The chip power consumption depends of the CSA bias current value which is tunable by an external resistor and a bit of slow control (state1<0>). It also depends on the value chosen to optimize the readout of the analog data (bias of the output buffers).

The nominal value of a CSA bias is ***400 µA*** and gives power consumption per channel around ***8 mW***; ***9.5 mW*** if this current is doubled.

11. The DC voltage and current references

11.1 DC voltage references

The AGET chip uses a number of DC reference voltages to polarize the input or output of a number of functionality as:

- The CSA DC output voltage
  [Vdc_csad/pin 133; Vdc_csag/pin 148],
- The PZ & SK filter DC output voltages
  [Vdc_cd/pin 134; Vdc_cg/pin 147],
- The Gain -2 DC output voltage
  [Vdc_g2d/pin 135; Vdc_g2g/pin 146],
- The Gain-2 & SCA DC reference voltages
  [Vref_scad/pin 138; Vref_scag/pin142],
- The common mode input voltage of the readout buffer
  [Vicm/pin 71],
- The common mode output voltage of the readout buffer
  [Vocm/pin 68].

Except for Vocm, all the others reference voltages are defined inside the chip and are adapted by Slow Control to the detector input signal polarity. For high frequency noise reduction, all the pads must be bypassed to ground by a 100 nF ceramic capacitor.

11.2 DC current references

Some bias currents must be defined externally on the PCB board. This is the case for those of:

- The CSA input transistor,
  [Ipol_csad/pin 126; Ipol_csag/pin 155]
- The input & output stages of the output buffer.
  [Vgg1/pin 69; Vgg7/pin 70]

All these currents can be defined using resistor connected between the bias pin and the ground (**Fig. 32**). Inside the chip, a PMOS transistor, with source connected to Vdd and with the gate and drain connected to the pin is defining the bias current. For optimum noise performances, the pin voltage should be bypassed to the Vdd used to supply the block biased by the reference.

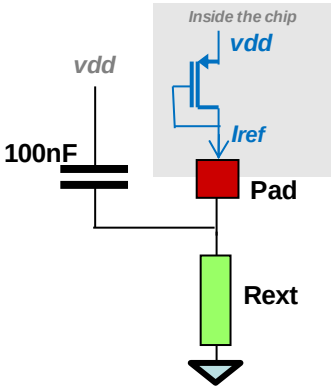


Fig. 32: Principle of external bias current reference.

To minimize the parasitic coupling effect of the channel CSA saturation, a 100 nF ceramic capacitor must be put to the 4 C_Ipol_csag&d pins [pins: 17; 34; 87 & 104]. These 4 pins give access to the voltage reference Ipol_csad & Ipol_csag inside the ASIC and permit therefore to have better voltage stabilization.

11.2.A Input transistor bias current of the CSA

This current value can be tuned to minimize the noise. The tuning range extends from 200 µA to 1 mA. A Rext resistor of 5.1 K set the bias current of the CSA to 400 µA (or 800 µA if the slow control bit doubling this current is set to “1”).

11.2.B Input&output stage bias currents of the output buffer

The default values are reported in table 41. The value of Vgg7 can be extended to obtain a good settling time when the outputs will be loaded by the ADC.

N° pin	Name	Rext value	Current value	Description
69	**Vgg1**	***1.24 K***	***2 mA***	***Current bias for the input stage***
70	**Vgg7**	***2 K***	***1 mA***	***Current bias for the output stage***

Table 41: Pins setting the input & output bias currents of the output buffer.

11.2.C Vb_ra&Vbf pins

The two pins Vb_ra [pin 139] & Vbf [pin 143] provide the possibility to modify the internal current value of the SCA readout buffers. By default, these pins must be just bypassed to ground by a 100 nF ceramic capacitor.

12. The AGET main simulated characteristics

This chapter reports the main expected performances of the AGET chip. All data, obtained by simulation, are provided as reference.

12.1 Power consumption

The chip power consumption depends of the CSA bias current value which is tunable by an external resistor and a bit of slow control (state1<0>). It also depends on the value choose to optimize the readout of the analog data (bias of the output buffers).

For a CSA bias value of ***400 µA***, the power consumption per channel will be around ***8 mW***, ***9.5 mW*** if this current is doubled.

12.2 Charge transfer function

The AGET circuit transfer function can be expressed as:

$$FDT = F_{CSA}.G_{Chain} \qquad \text{(eq. 1)}$$

Where:

- F_{CSA} is the transfer function of the CSA (CSA output voltage divided by input charge V/C),
- G_{Chain} is the voltage gain of the whole analog chain from the CSA output to the chip output.

The F_{CSA} depends on the chip range, the detector capacitance and on the CSA bias current. The G_{Chain} is nearly constant but is slightly dependent on the peaking time value and of the integration time of the detector signal. The simulated transfer functions for different conditions are plotted in the **Fig. 33** to the **Fig. 40**.

The decrease of the transfer function with detector capacitor is higher for the lowest peaking times due to an increase of the CSA rise time and therefore responsible of ballistic deficit.

This decrease can be reduced by applying a higher current value in the CSA input transistor.

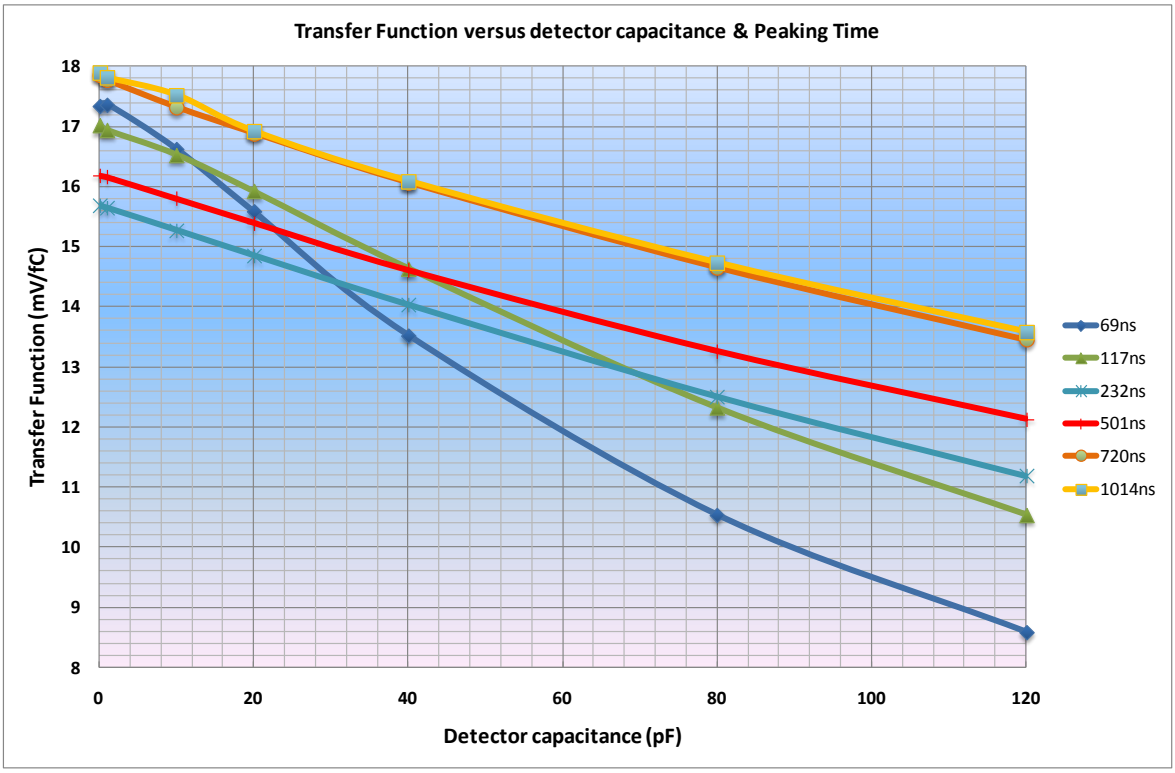


Fig. 33: Simulated transfer functions vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 400µA.

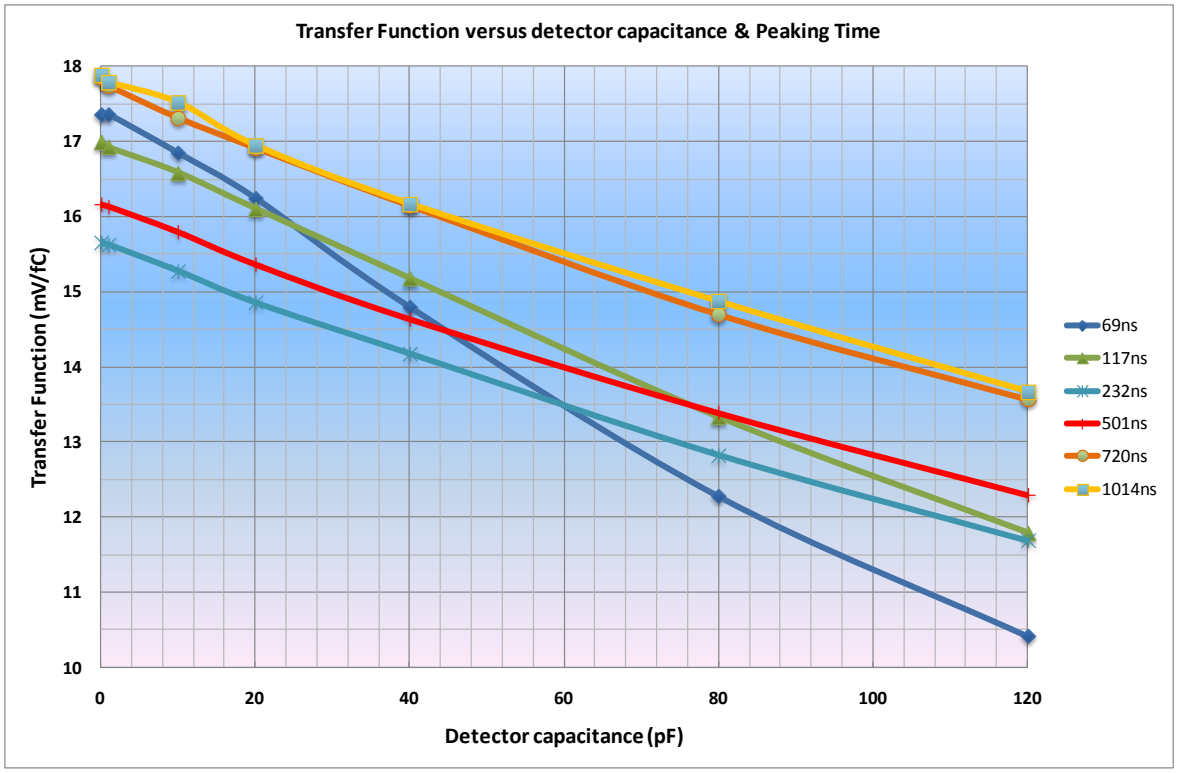


Fig. 34: Simulated transfer functions vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 800µA.

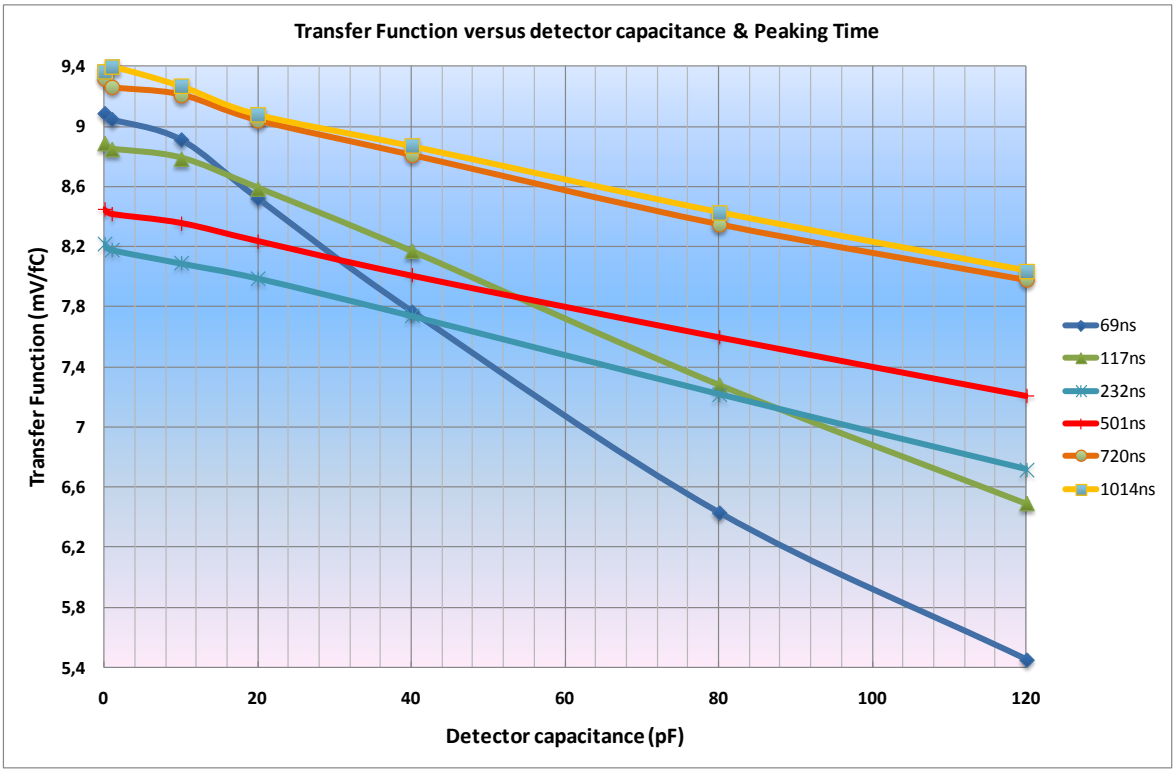


Fig. 35: Simulated transfer functions vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 400µA.

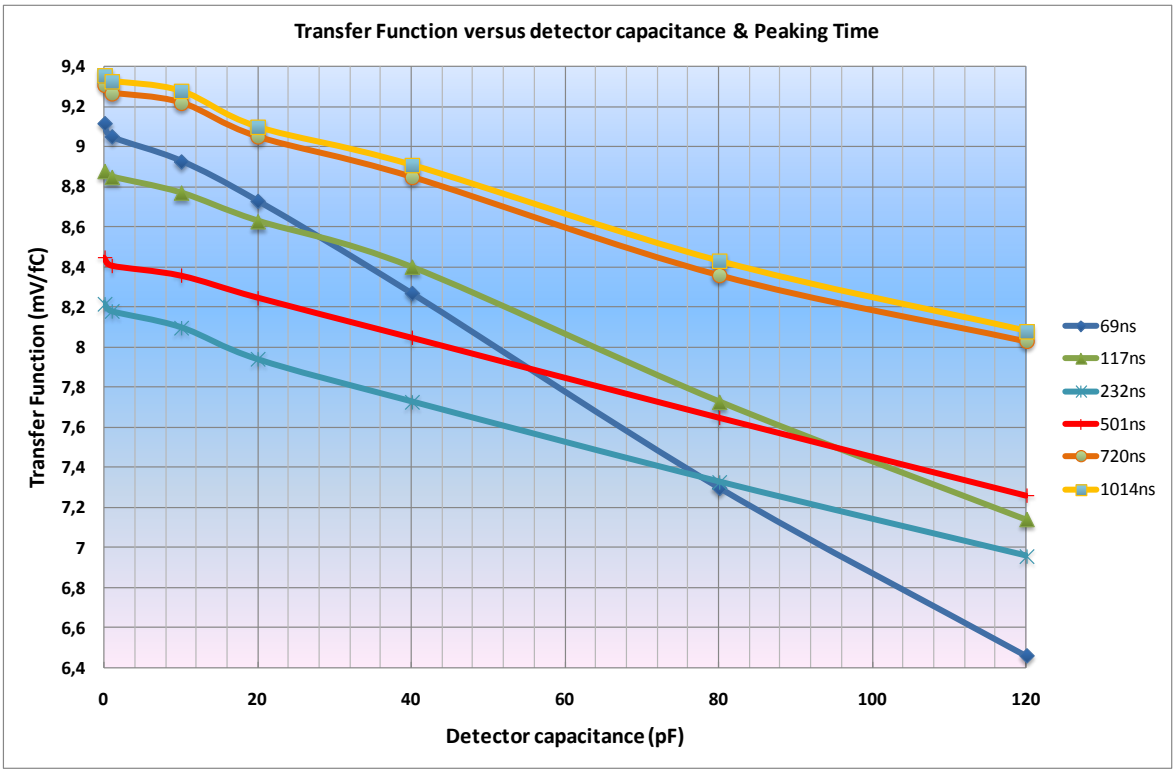


Fig. 36: Simulated transfer functions vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 800µA.

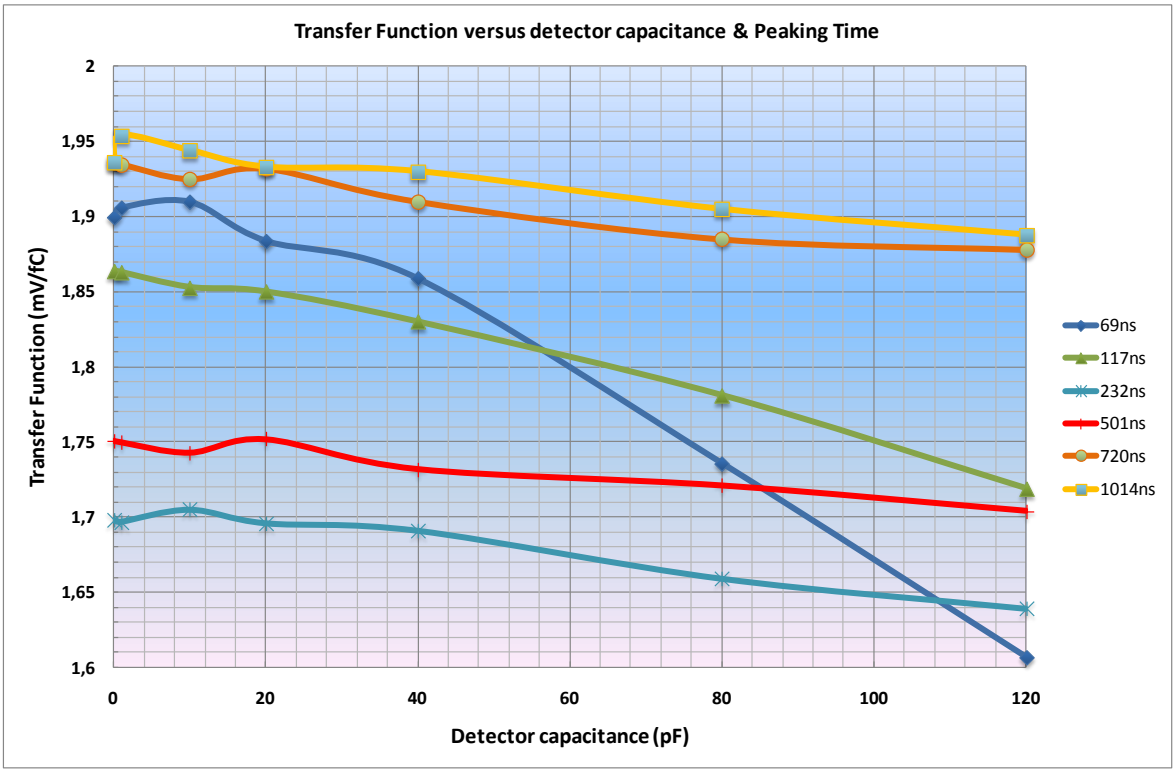


Fig. 37: Simulated transfer functions vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 400µA.

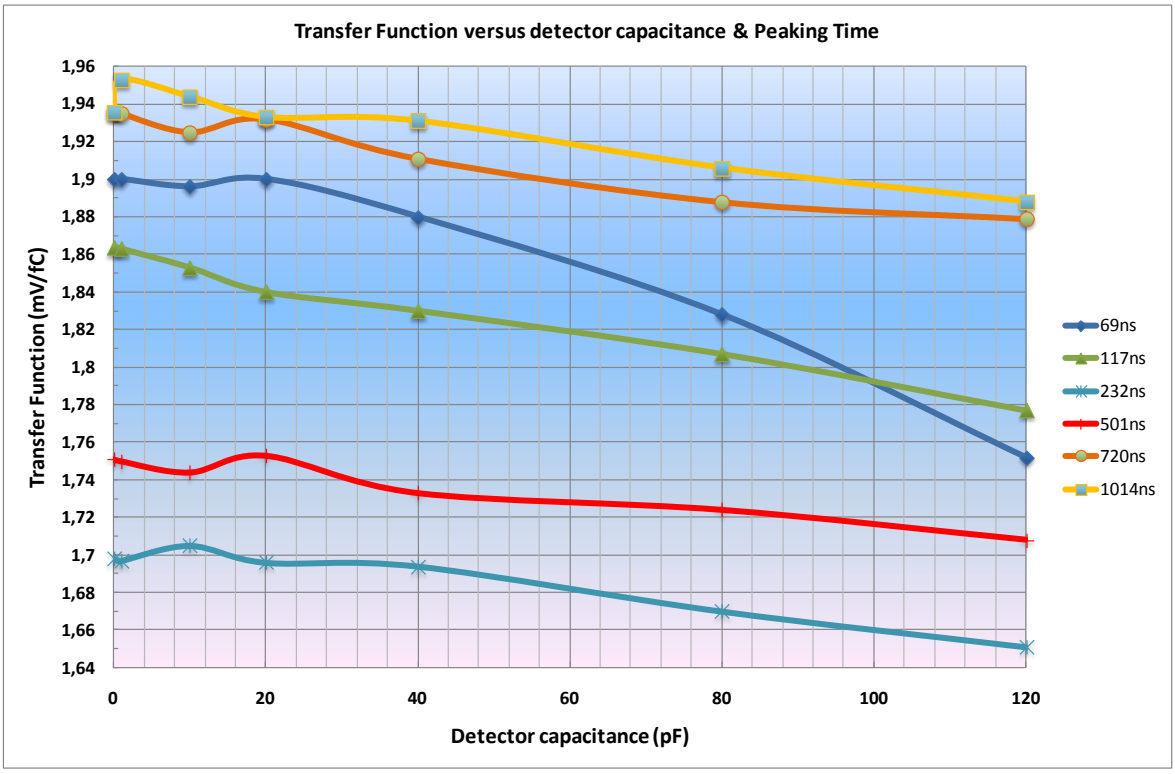


Fig. 38: Simulated transfer functions vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 800µA.

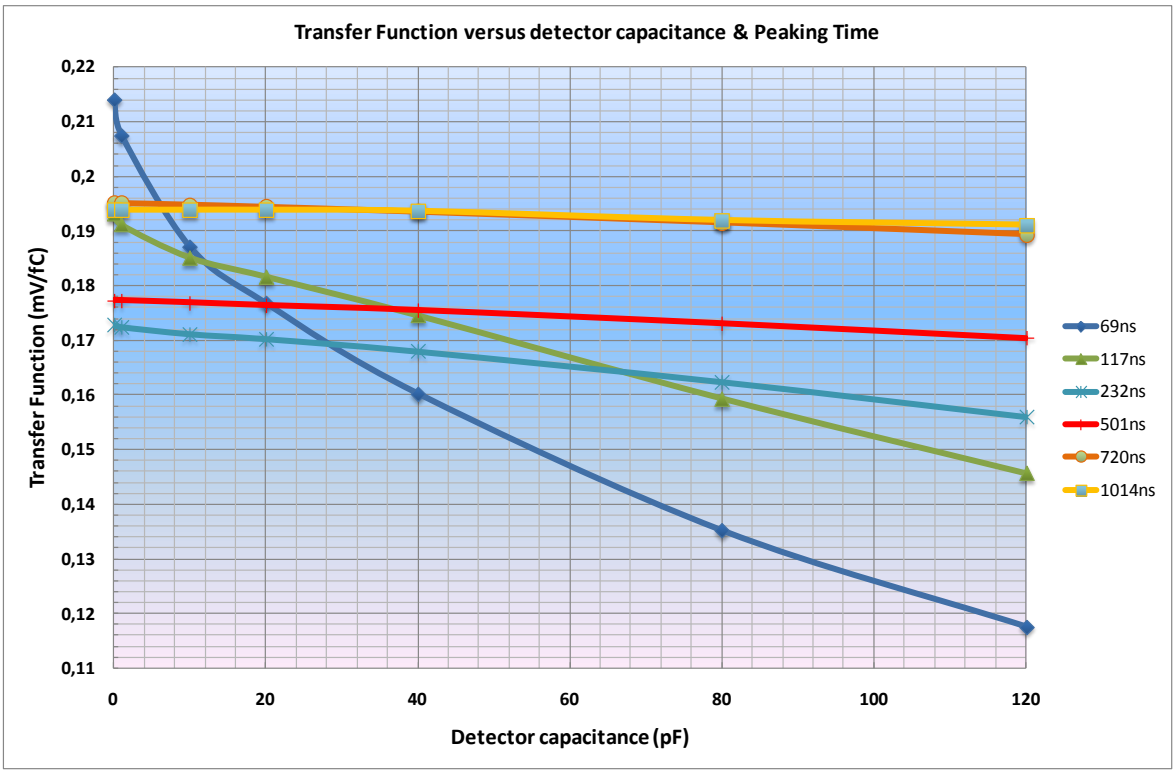


Fig. 39: **Simulated transfer functions vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 400µA.**

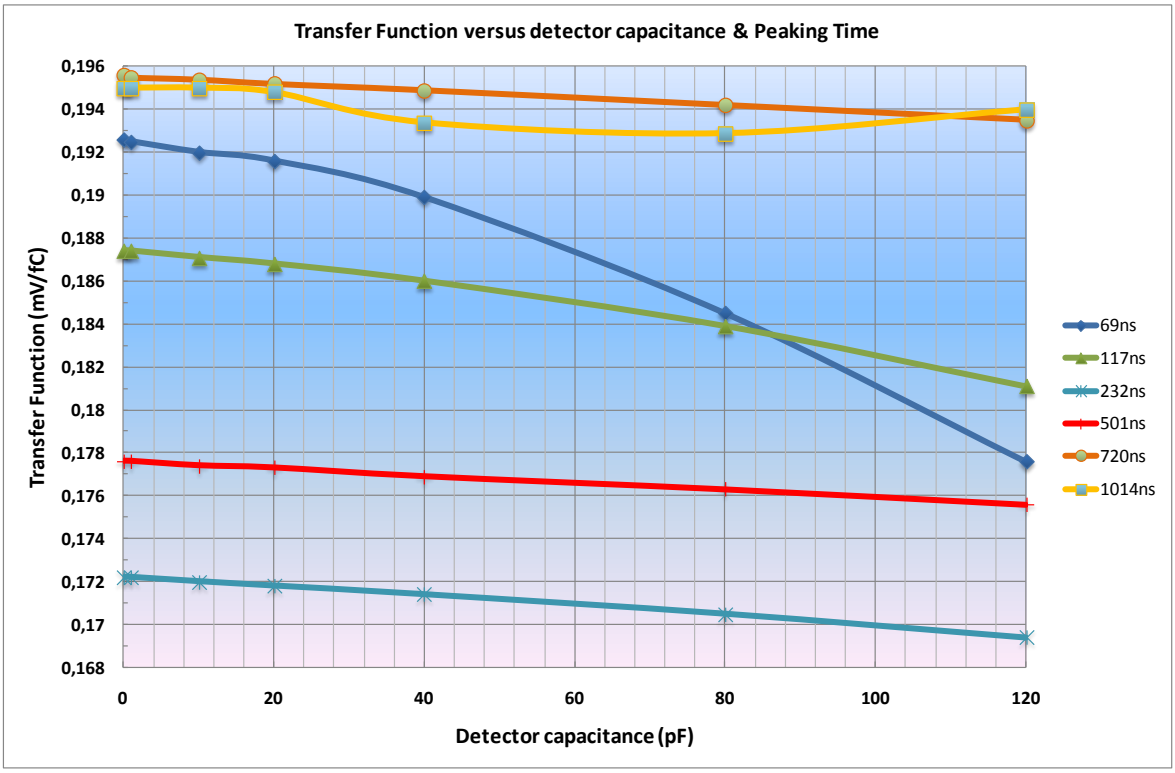


Fig. 40: **Simulated transfer functions vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 800µA.**

12.3 The charge Signal over Noise ratio

This chapter describes the effect of the different noise sources on the charge measurement.

12.3.A Channel noise

The Equivalent Noise Charge (ENC) is calculated as:

$$\mathbf{ENC^2_{AGET}} = ENC^2_{CSA} + V^2_{n\_2ndStage}/FDT^2 \qquad \text{(eq. 2)}$$

Where:

- ENC^2_{CSA} is the CSA contribution to the ENC^2_{AGET},
- $V^2_{n\_2ndStage}$ is the rms noise voltage measured at the chip output corresponding to the noise contribution of all the blocks excepted the CSA,
- FDT is the transfer function of the chip.

The ENC^2_{CSA} can be expressed as:

$$\mathbf{ENC^2_{CSA}} = ENC^2_{CSAserie} + ENC^2_{CSA1/f} + ENC^2_{CSA//} \qquad \text{(eq. 3)}$$

Where:

- $ENC_{CSAserie}$, $ENC_{CSA1/f}$ & $ENC_{CSA//}$ are respectively the serie, 1/f and parallel contributions to the ENC.

The FDT can be expressed as:

$$\mathbf{FDT^2} = F^2_{CSA120f}.G^2_{chain} / Range^2_{CSA} \qquad \text{(eq. 4)}$$

Where:

- $F_{CSA120f}$ is the transfer function of the CSA in the 120 fC range,
- $Range_{CSA}$ is the "range ratio" of the CSA (1 for 120 fC range, 2 for 240 fC, 8.33 for 1 pC range and 83.33 for 10 pC range).

Finally, the ENC_{AGET} expression in (2) can be described by taking (3) & (4) as:

$$ENC^2_{AGET} = \alpha^2_{Ipolcsa}.(C_0 + C_{in})^2/t_p + \gamma^2.(C_0 + C_{in})^2 + \beta^2.t_p + V^2_{n\_2ndStage}.Range^2_{CSA}/(F^2_{CSA120f}.G^2_{Chain}) \qquad \text{(eq. 5)}$$

Where:

- $\boldsymbol{\beta}$ is a constant for parallel noise (depending on the CSA feedback and on the detector anode bias resistor),
- $\boldsymbol{\gamma}$ is constant for 1/f noise (depending on the CSA input transistor and weakly on the CSA bias current),
- $\boldsymbol{\alpha}$ is for the serie noise contribution. It mainly depends on the CSA input transistor and it is varying as I^{-A}_{polcsa}, where I_{polcsa} is the CSA input transistor bias current and A the coefficient in the range of 0.25 to 0.5 depending on the inversion level of the input transistor,
- $\boldsymbol{C_0}$ is the chip input capacitor (including the capacitors of the input device, internal protection network and of the package),
- $\boldsymbol{C_{in}}$ is the capacitor connected externally to the chip input (including those of the detector, PCB, connectors and parasitic elements).

For the detector capacitor and shaping time ranges of the application, the parallel noise contribution is supposed to be negligible. Therefore, the noise will be mainly due to 3 contributions:

- The serie one, which will be the highest for short shaping times and large input capacitors. It can be decreased by increasing the I_{polcsa} value,
- The 1/f noise which scales with the input capacitor, but is independent of the shaping time. It will probably be not negligible for large input capacitors and slow shaping,
- The "second stage" contribution, independent of the shaping, but that increases for the largest ranges. It will dominates in the following cases:
    - Largest charge ranges,
    - Slow shaping times with relatively small input capacitor.

  In these cases, the noise will be nearly independent of the shaping time.

The $V^2_{n\_2ndStage}$ contribution is the quadratic sum of the several terms:

- V_{ADC} = *195 µV rms (0.4 ADC_u):* ADC noise (from the datasheet),
- V_{Buffer} = *275 µV rms (0.56 ADC_u):* Differential output buffer,
- $V_{SCAread}$ = *100 µV rms (0.2 ADC_u):* Total contribution for SCA readout,
- V_{SCAfpn} = *537 µV rms (1.1 ADC_u):* SCA fixed pattern noise (AFTER measurements),
- $V_{G=2;Buffer}$ = *380 µV rms (0.78 ADC_u):* -2 buffer contribution,
- $V_{Filters}$ = *780 µV rms (1.6 ADC_u):* Filters noise (PZC + Sallen-key).

Thus:

- The simulated total "second stage" contribution is: 1.07 *mV rms (2.2 ADC_u), 940 µV rms (1.9 ADC_u)* without the fixed pattern noise,
- The simulated noise of the multiplexer, the output buffer and the ADC is: *350 µV rms (0.72 ADC_u),*
- The simulated noise for the "FPN" channel is: *525 µV rms (1.01 ADC_u)* and becomes 751 *µV rms (1.54 ADC_u)* if the fixed pattern noise contribution is included.

To calculate the ENC due to these contributions, they should be renormalized by the transfer function of the chain ($Range_{CSA}/(F_{CSA120f}.G_{Chain})$ (in equation (5)). Table 42 summarizes the mean transfer function for the 4 ranges (that actually are depending (+/- 10%) of the peaking time > 50ns, the CSA input current and the detector capacitor < 40pF).

Charge range (fC)	Transfer function (mV/ke-)	Total second stage noise contribution to ENC (e- rms) including FPN	Total second stage noise contribution to ENC (e- rms) without FPN
120	***2.61***	***410***	***360***
240	***1.39***	***769***	***676***
1000	***0.29***	***3690***	***3241***
10,000	***0.029***	***36896***	***32413***

Table 42: Transfer function and second stage contribution for the 4 charge ranges.

The simulation results for the different parameters in each charge range are plotted in the **Fig. 41** to the **Fig. 48**.

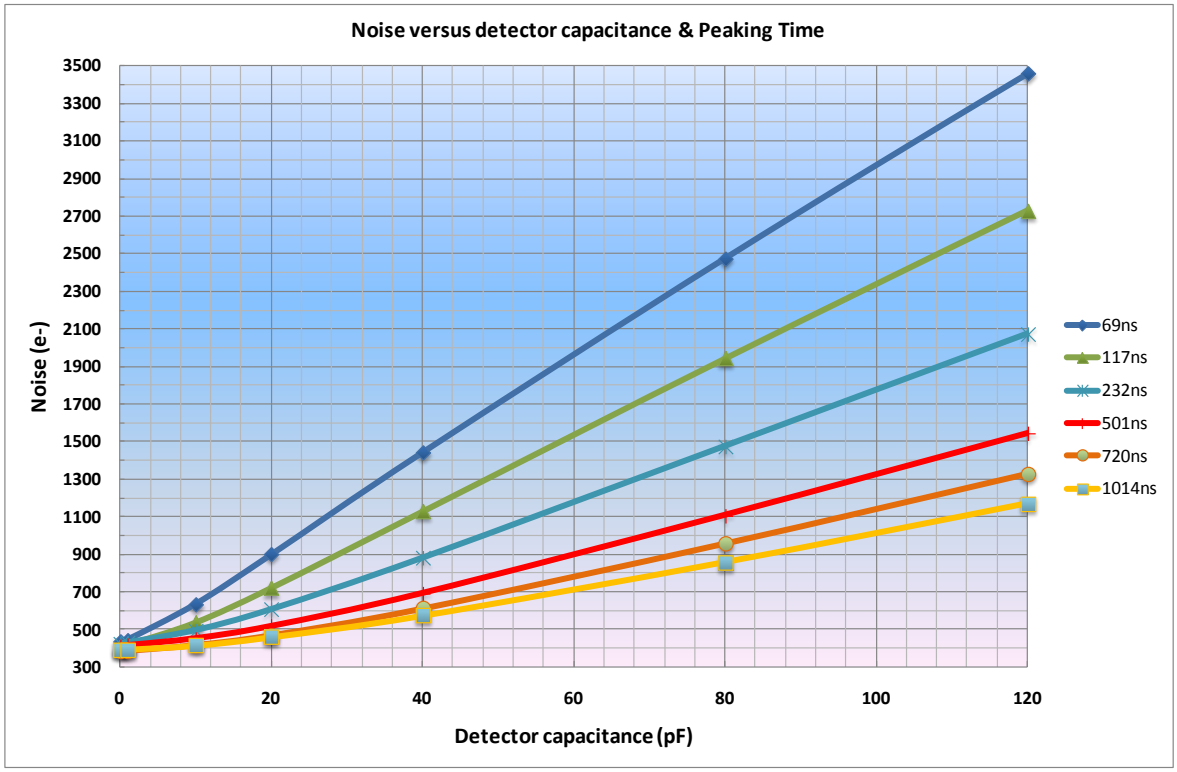


Fig. 41: **Simulated *ENC(Cin,tp)* in the 120 fC range for Icsa = 400 µA.**

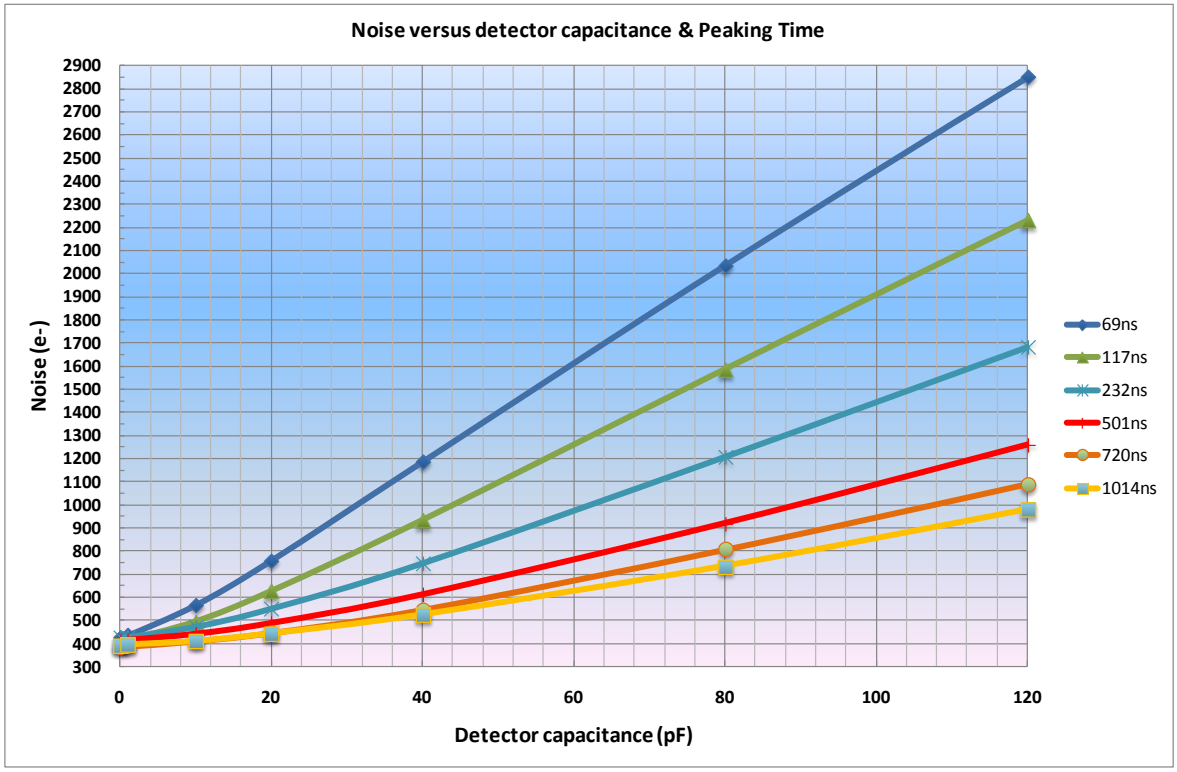


Fig. 42: **Simulated *ENC(Cin,tp)* in the 120 fC range for Icsa = 800 µA.**

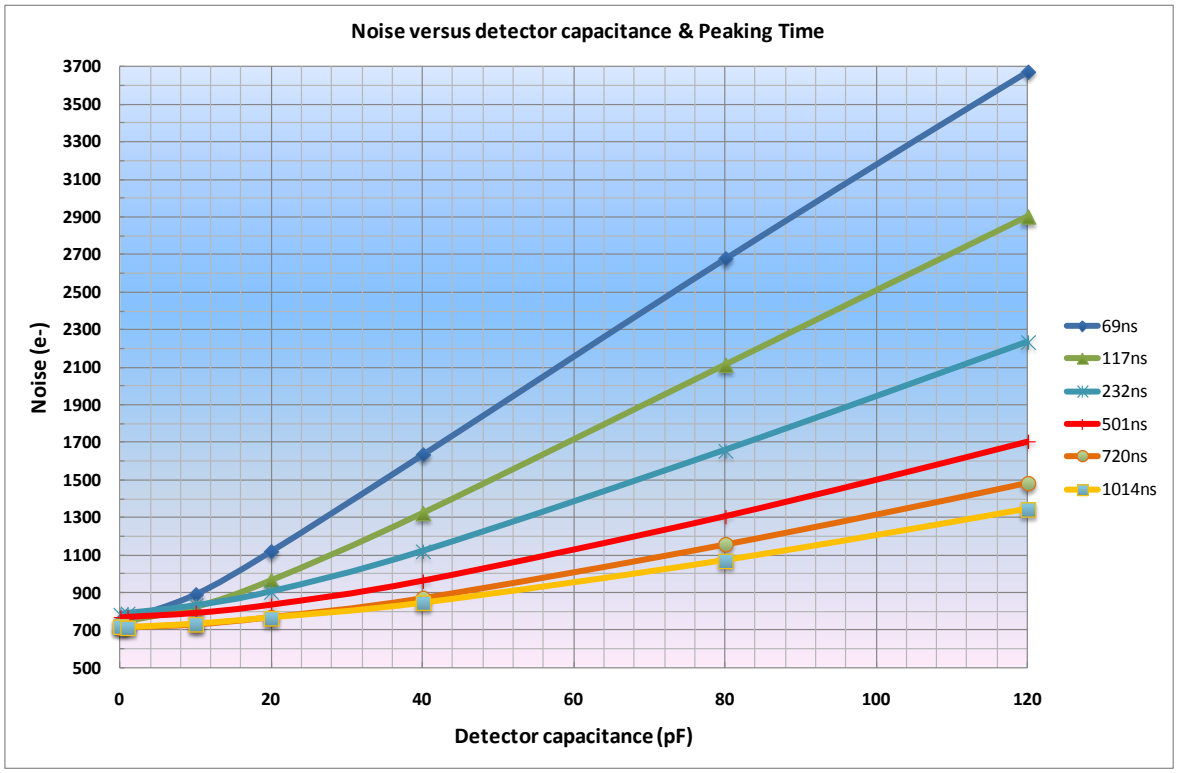


Fig. 43: **Simulated $ENC_{(Cin,tp)}$ in the 240 fC range for Icsa = 400 µA.**

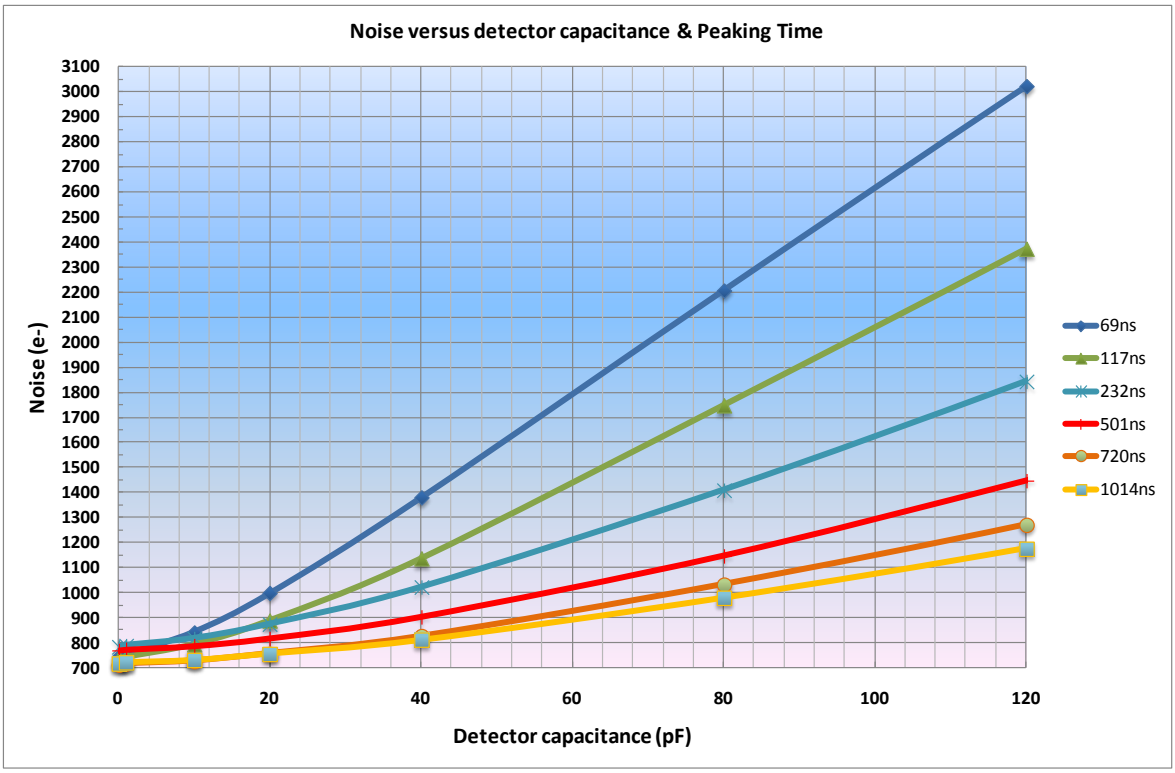


Fig. 44: **Simulated $ENC_{(Cin,tp)}$ in the 240 fC range for Icsa = 800 µA.**

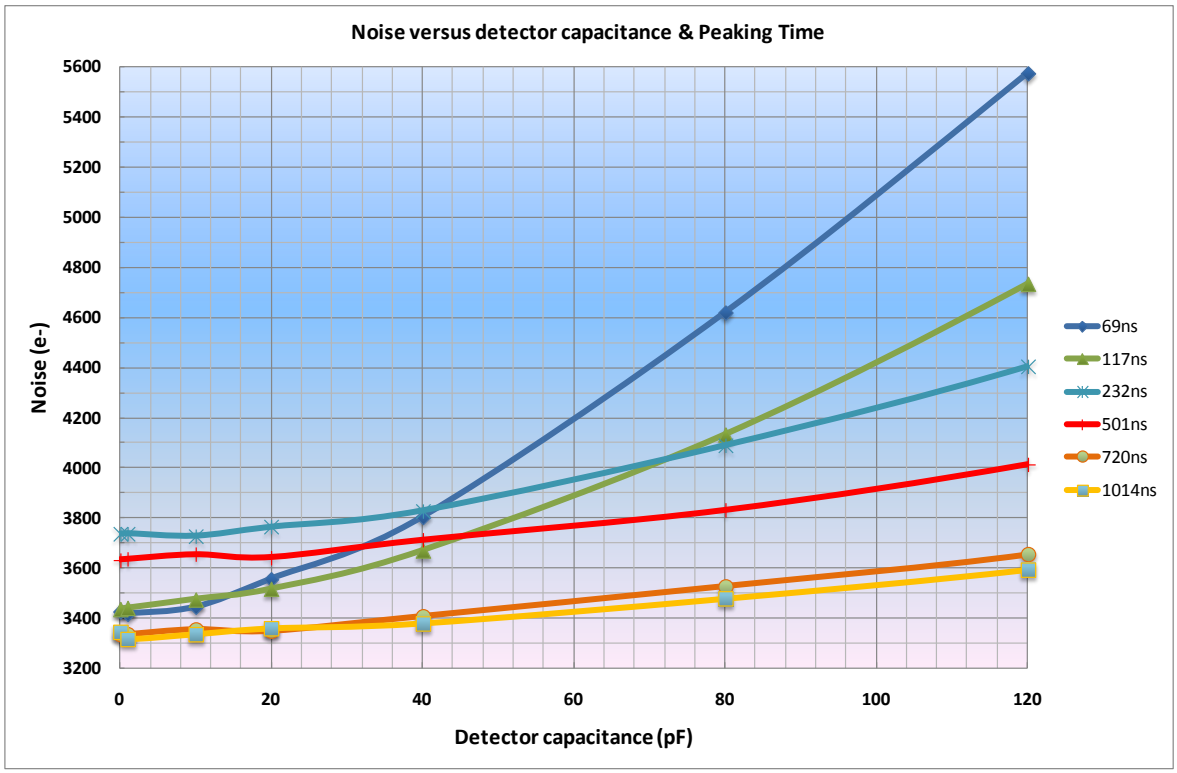


Fig. 45: **Simulated $ENC_{(Cin,tp)}$ in the 1 pC range for Icsa = 400 µA.**

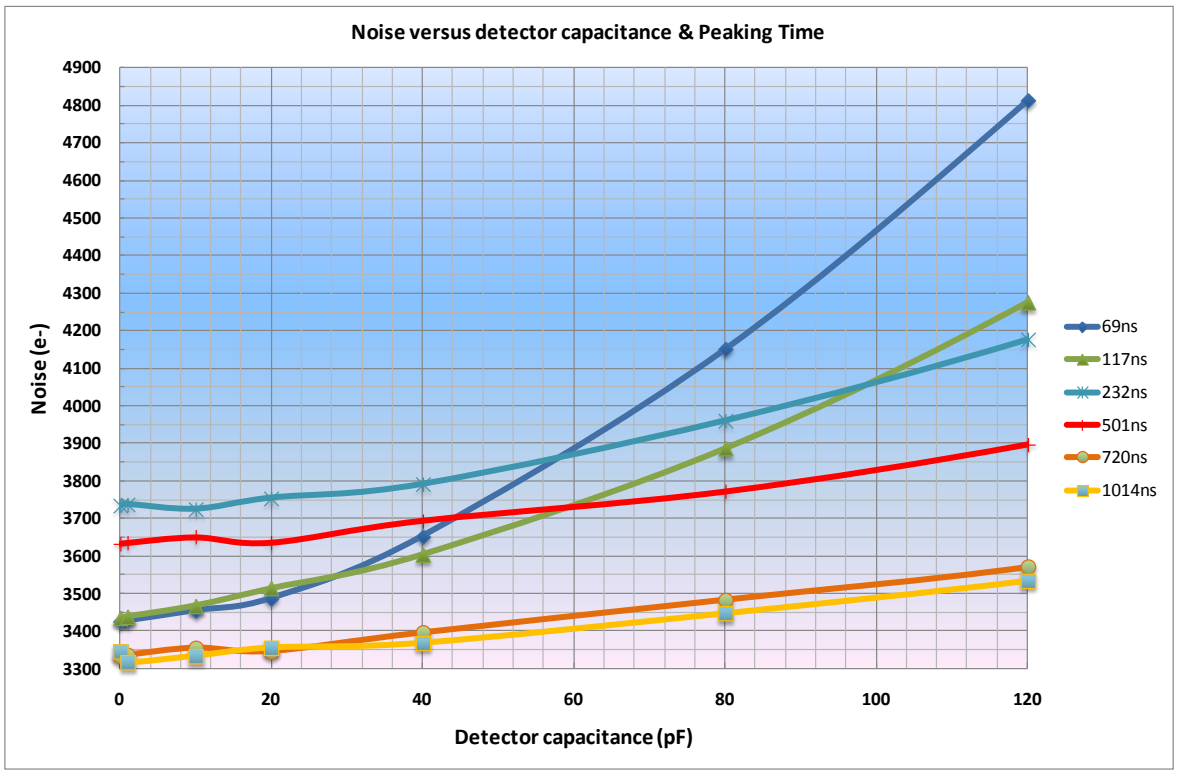


Fig. 46: **Simulated $ENC_{(Cin,tp)}$ in the 1 pC range for Icsa = 800 µA.**

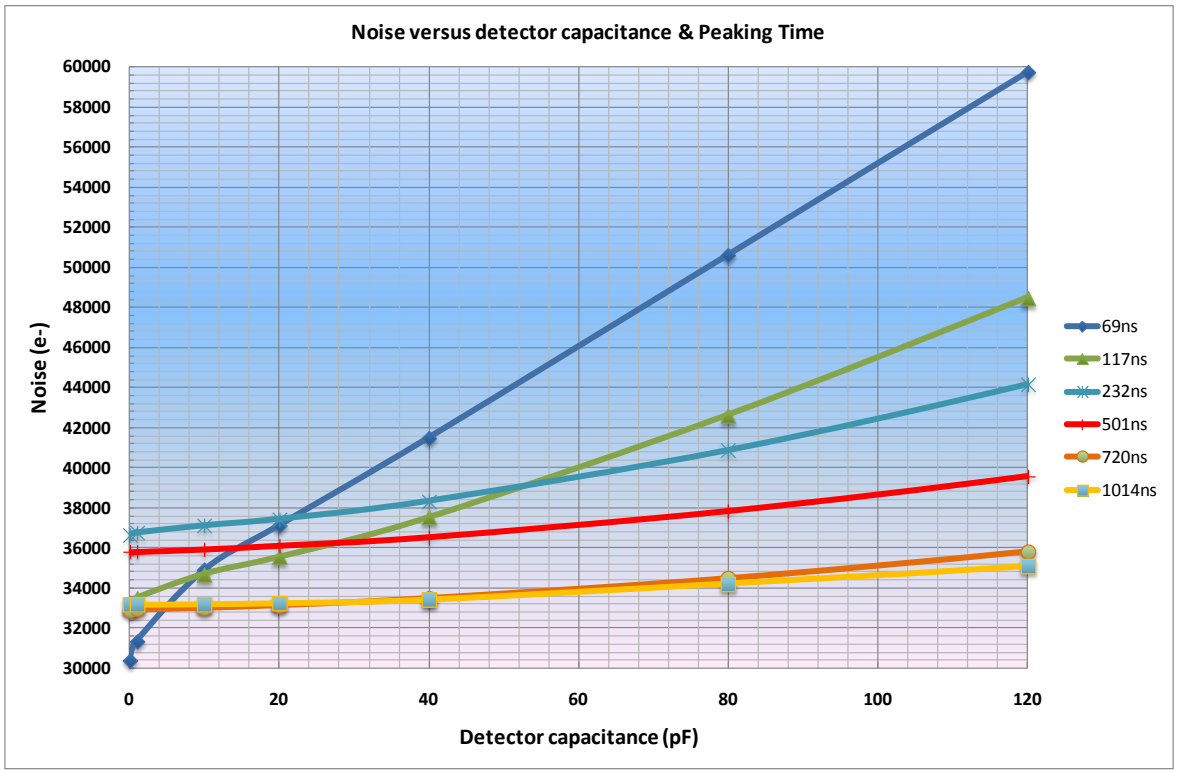


Fig. 47: **Simulated *ENC(Cin,tp)* in the 10 pC range for Icsa = 400 µA.**

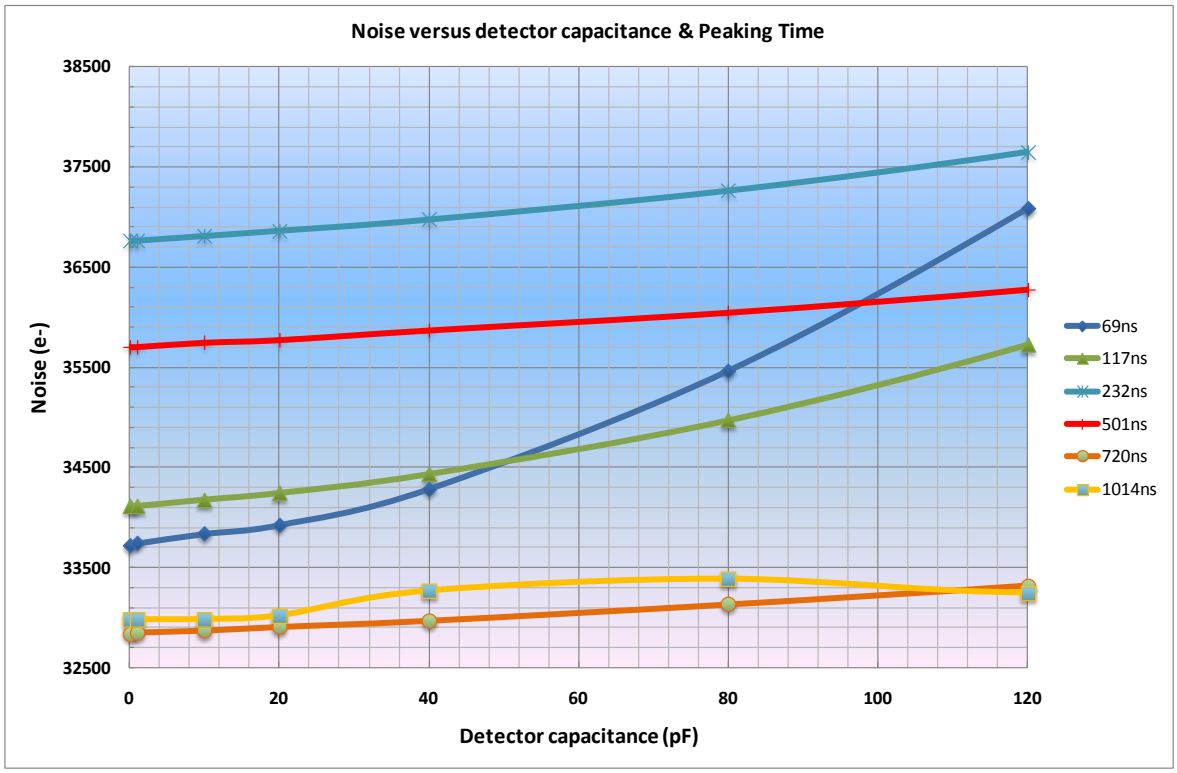


Fig. 48: **Simulated *ENC(Cin,tp)* in the 10 pC range for Icsa = 800 µA.**

12.3.B Fixed Pattern Noise (FPN)

The SCA channel is made of a row of storage capacitors addressed by MOS switches. It is well know that there is an offset spread between the capacitors of the same line: the offset of each capacitor depends on its index. The rms value of the spread of the mean baseline measured on each cell of the SCA channel is called the Fixed Pattern Noise (FPN). The FPN is mainly due to switching charge injection spread and to the spread in the sampling of parasitic signals propagating in the substrate or power supplies. Very often, the FPN pattern is very similar from channel to channel.

In standard mode of operation, the read operation can start at any cell of the SCA, so that the FPN is randomized and will appear as a noise (with a very large coherent part between channels).

Nether less, as the FPN is often very reproducible, it can be subtracted from output data. The **Fig. 49** to the **Fig. 51** give an example of measured pattern on several channels of AGET prototype version.

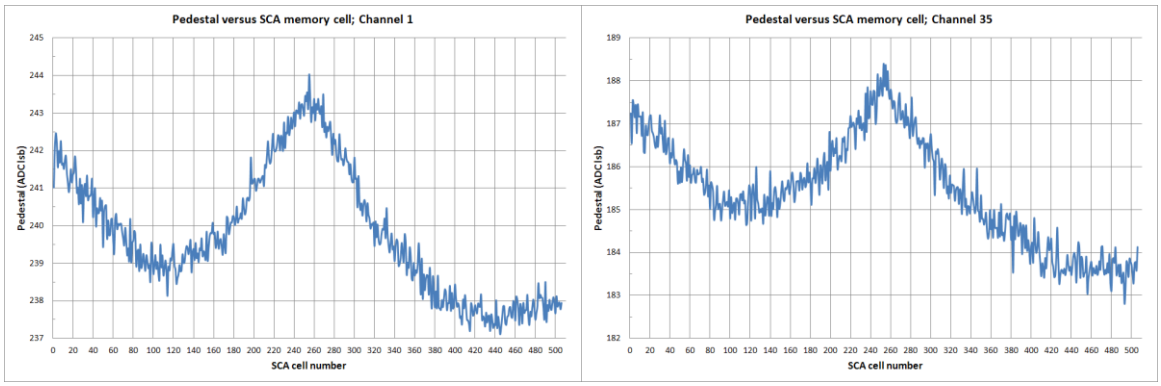


Fig. 49: **Pedestal versus memory cell. Channels 1 & 35.**

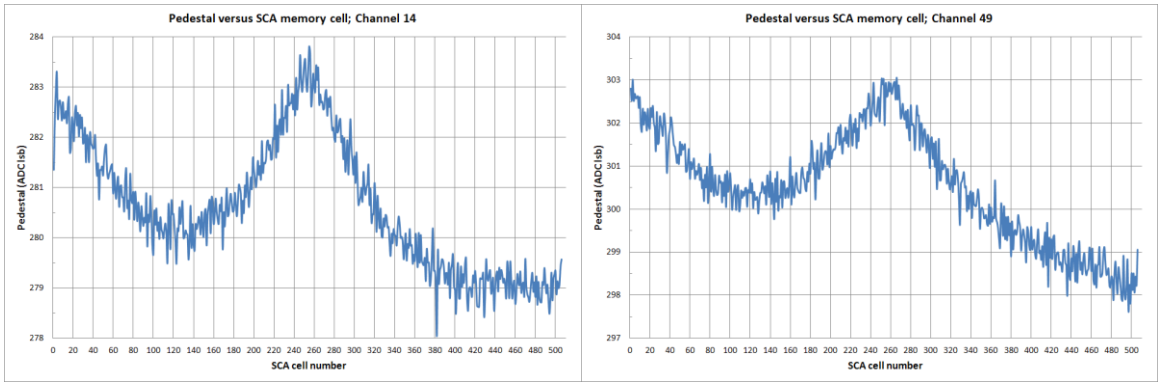


Fig. 50: **Pedestal versus memory cell. Channels 14 & 49.**

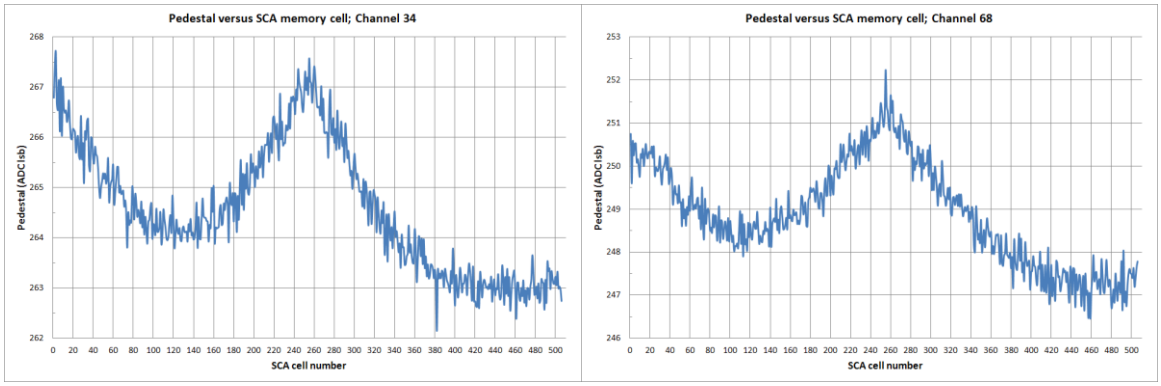


Fig. 51: **Pedestal versus memory cell. Channels 34 & 68.**

12.4 Signal shape

The SCA write frequency is adapted in order to match the SCA time range with the maximum drift time in the TPC. The peaking time of the filter must be adapted to match both detector signal and the SCA write frequency to keep enough samples for charge and time measurement.

The filter integrated in AGET is a CR-RC^2 with two complex poles providing a quasi-semi-Gaussian shape with less than 1% undershoot. The simulated timing parameters of the shaped signal are reported in the **Fig. 52**.

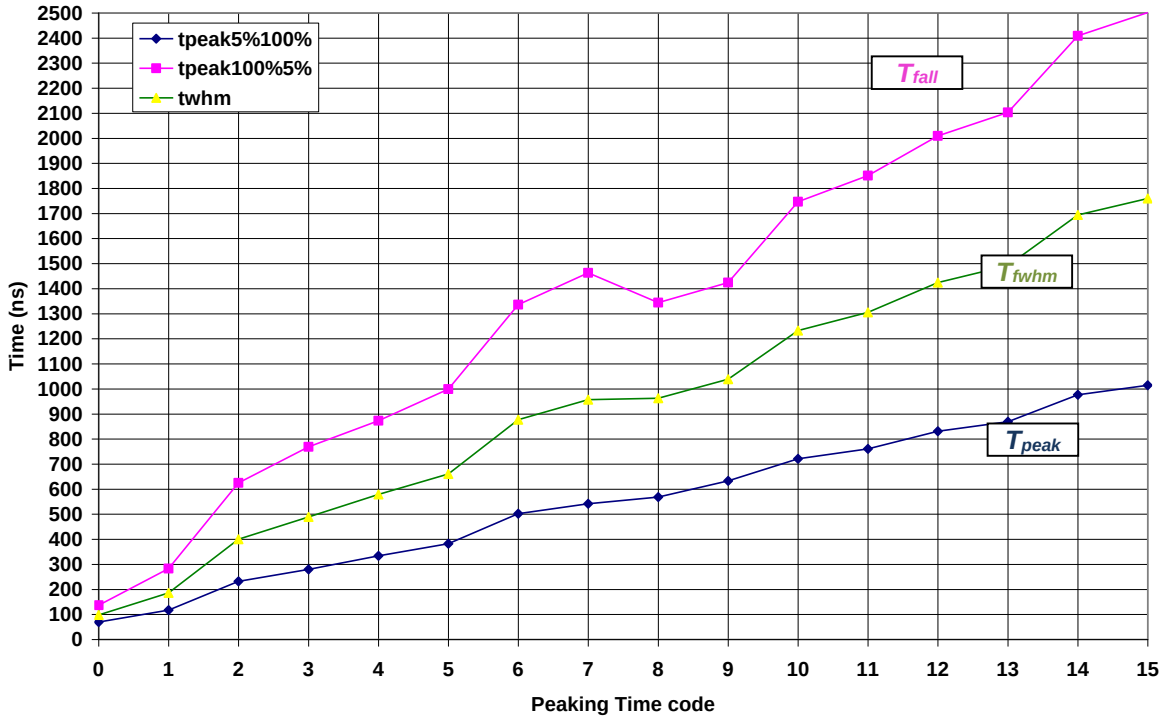


Fig. 52: **Time occupancy parameters of the filtered signal.**

In this figure, T_{peak} is the signal rise time measured from 5 % of the full amplitude to the peak, T_{fall} is the signal fall time measured from the peak to 5% of the full amplitude and T_{fwhm} is the signal width measured at 50% of the maximum signal amplitude.

12.5 Threshold channel

This part describes the main characteristics of the threshold channel as the transfer function, minimum and maximum threshold values.

12.5.A Input transfer function

The AGET circuit transfer function can be expressed as:

$$FDT = F_{CSA}.G_{ChainThreshold} \qquad \text{(eq. 6)}$$

Where:

- F_{CSA} is the transfer function of the CSA (CSA output voltage divided by input charge V/C),
- $G_{ChainThreshold}$ is the voltage gain of the whole analog chain from the CSA output to the discriminator input.

This gain can be adjusted by slow control to 5 or 17.5 % of the input dynamic range of the channel.

12.5.B Threshold transfer function

The threshold value is adjustable through 2 internal DACs:

- 3-bit DAC, common to all channels (+ 1 polarity bit), forms the MSB of threshold value,
- 4-bit DAC, one per channel, forms the LSB of threshold value.

The transfer function is plotted in the **Fig. 53**.

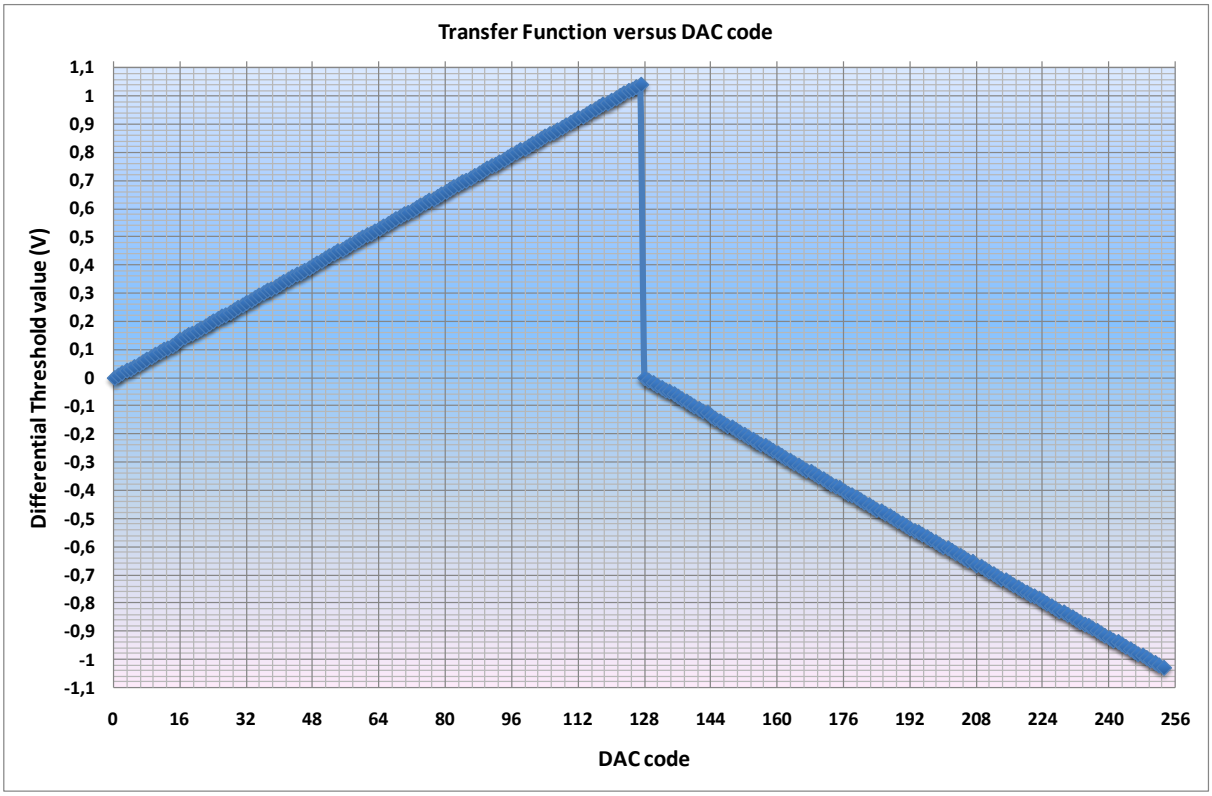


Fig. 53: Differential threshold value versus DAC code.

12.5.C Minimum threshold value at 5% of input dynamic range

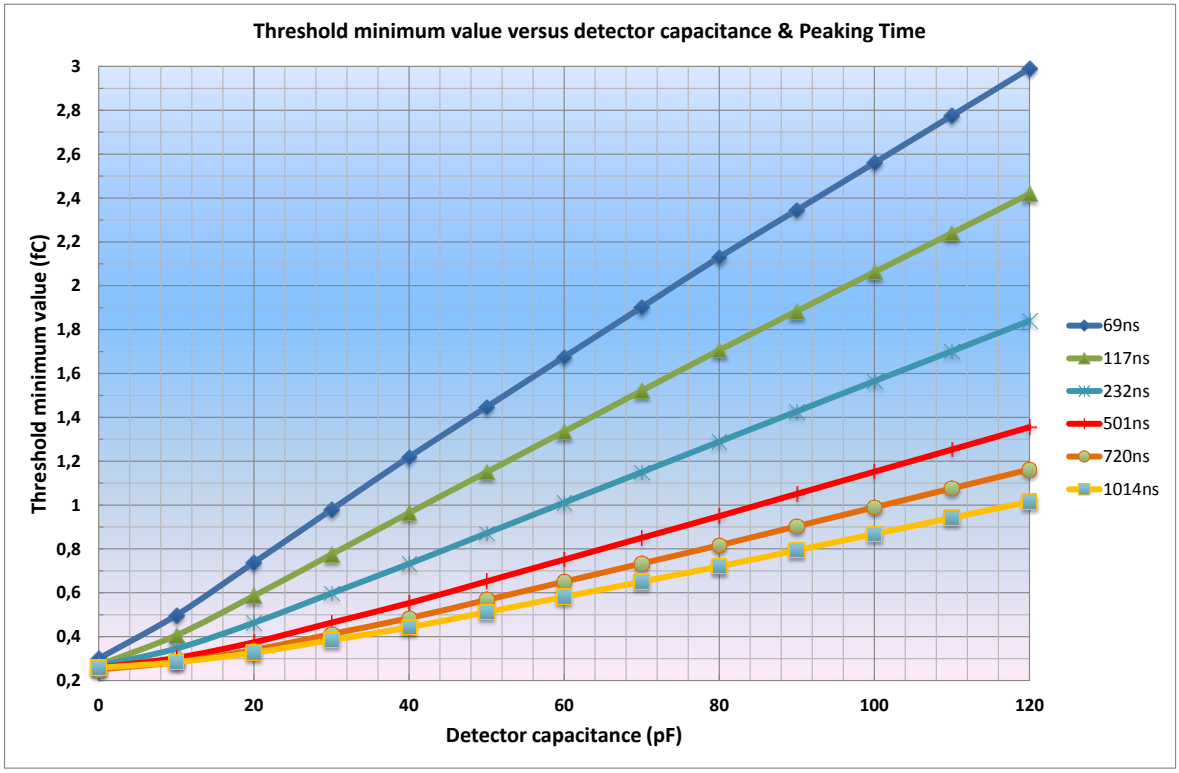


Fig. 54: Minimum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 400µA.

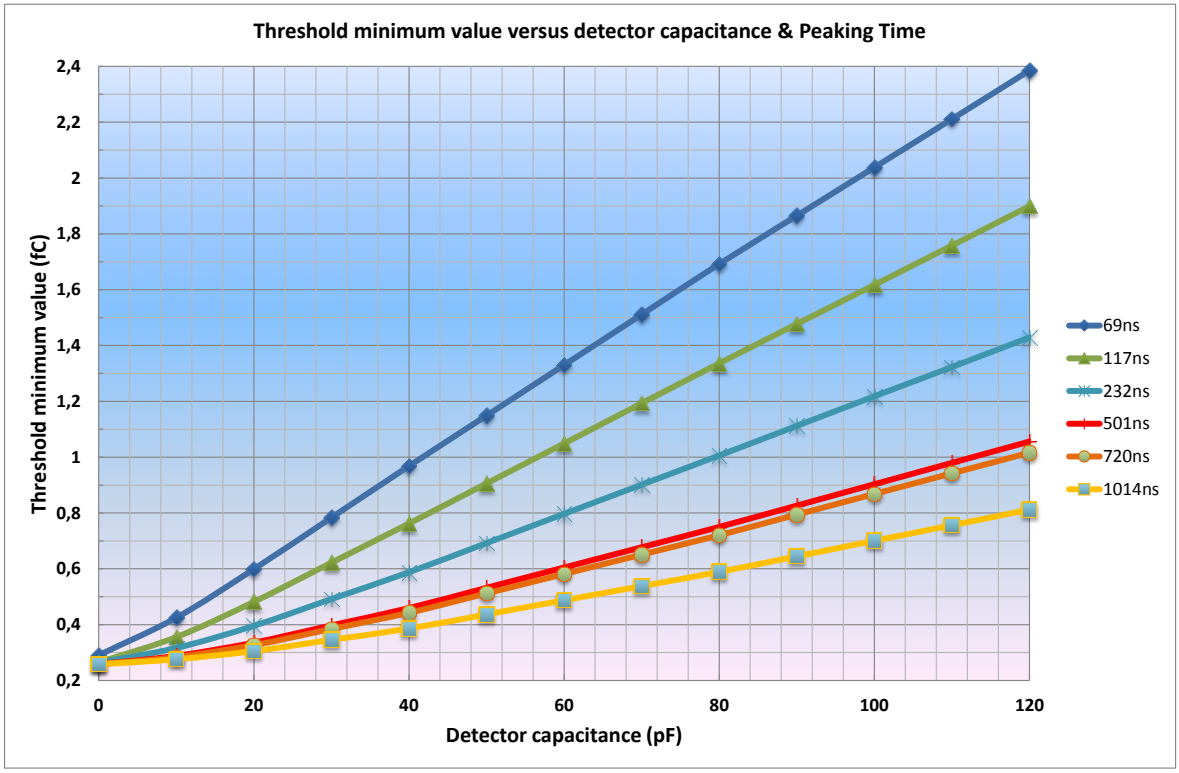


Fig. 55: Minimum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 800µA.

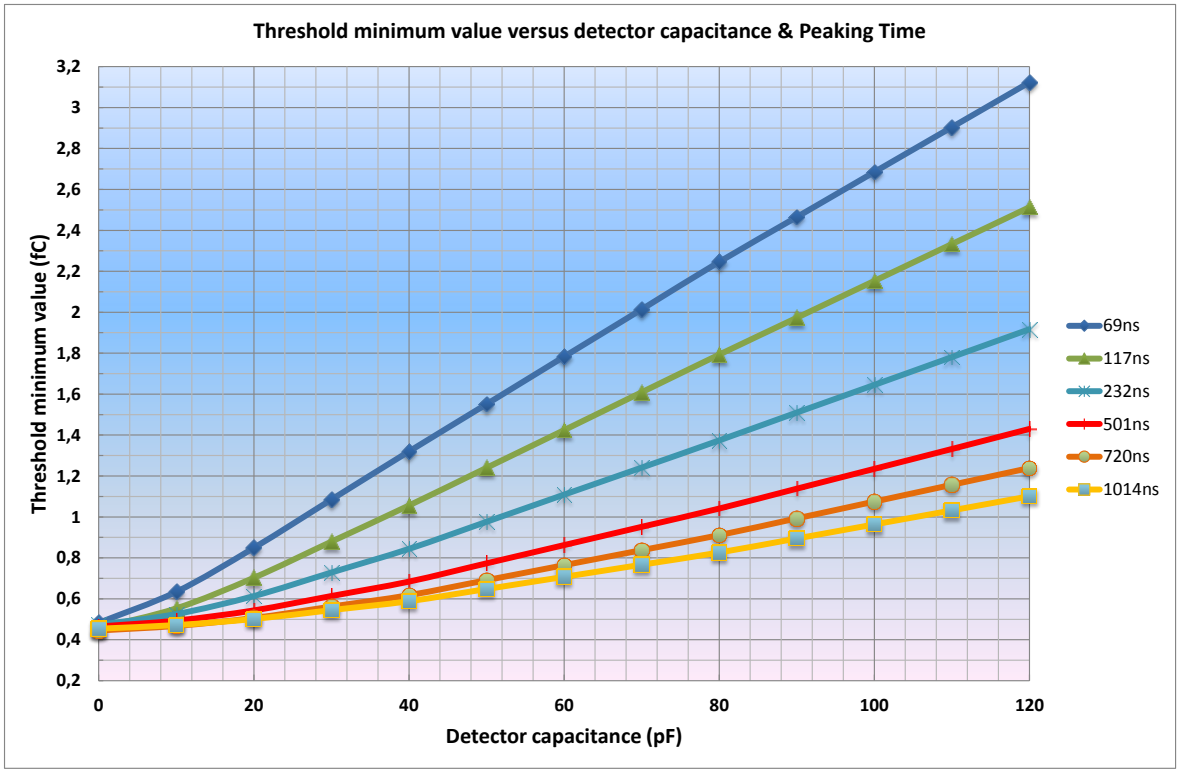


Fig. 56: Minimum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 400µA.

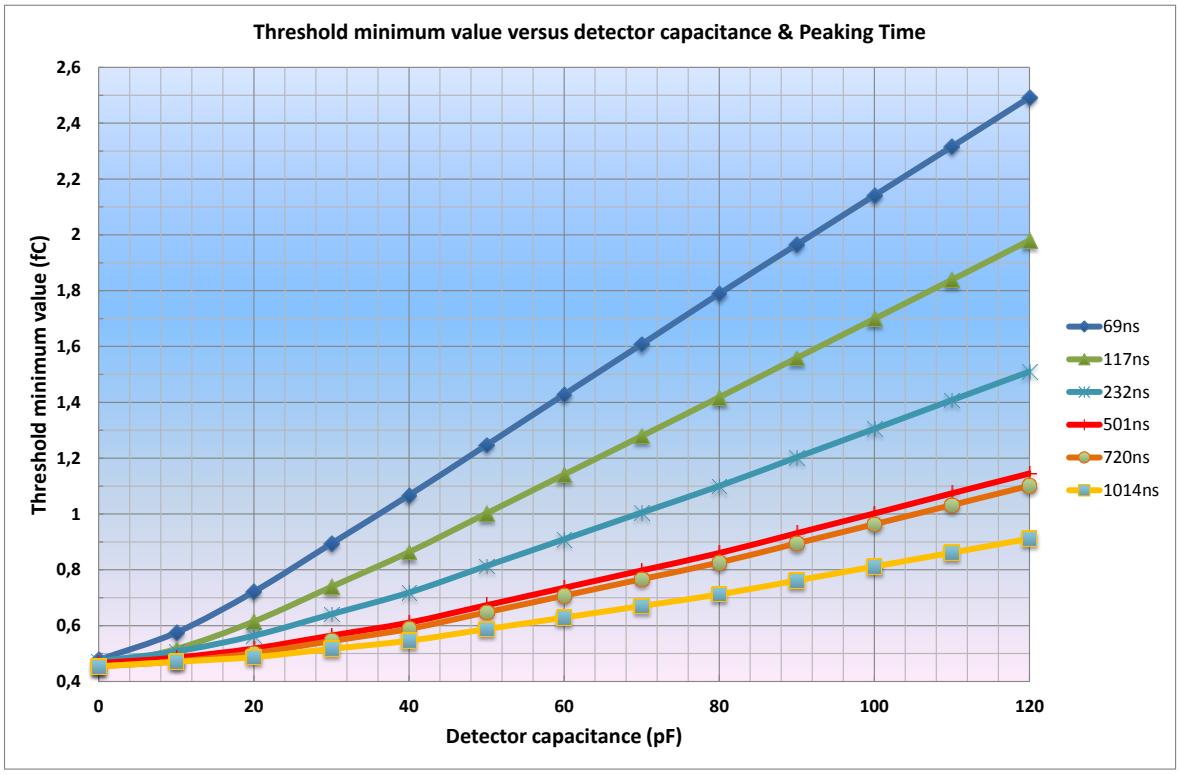


Fig. 57: Minimum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 800µA.

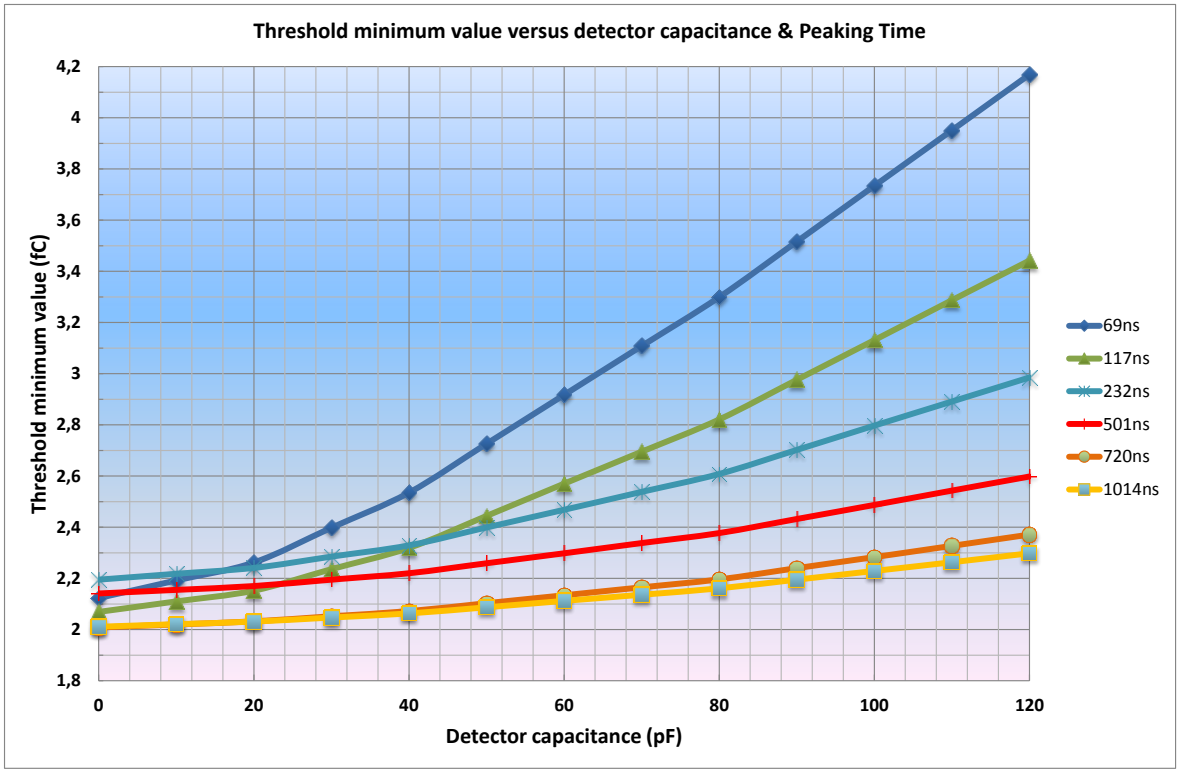


Fig. 58: Minimum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 400µA.

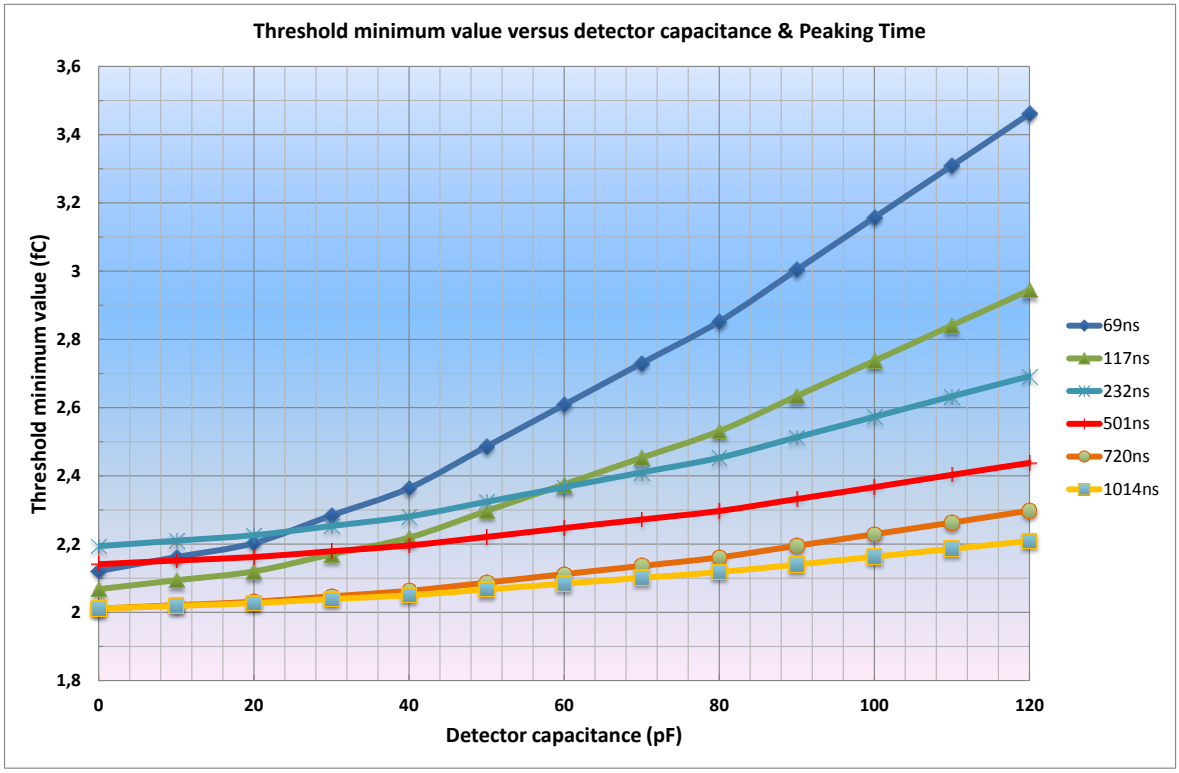


Fig. 59: Minimum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 800µA.

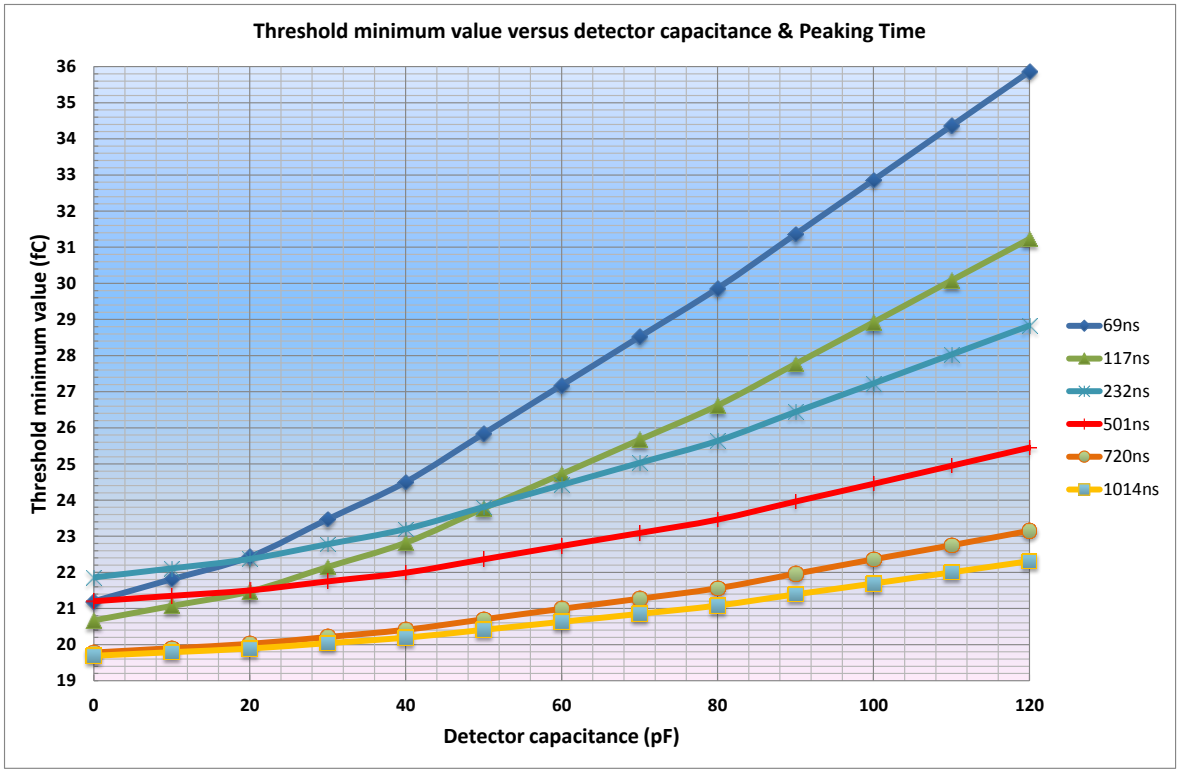


Fig. 60: Minimum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 400µA.

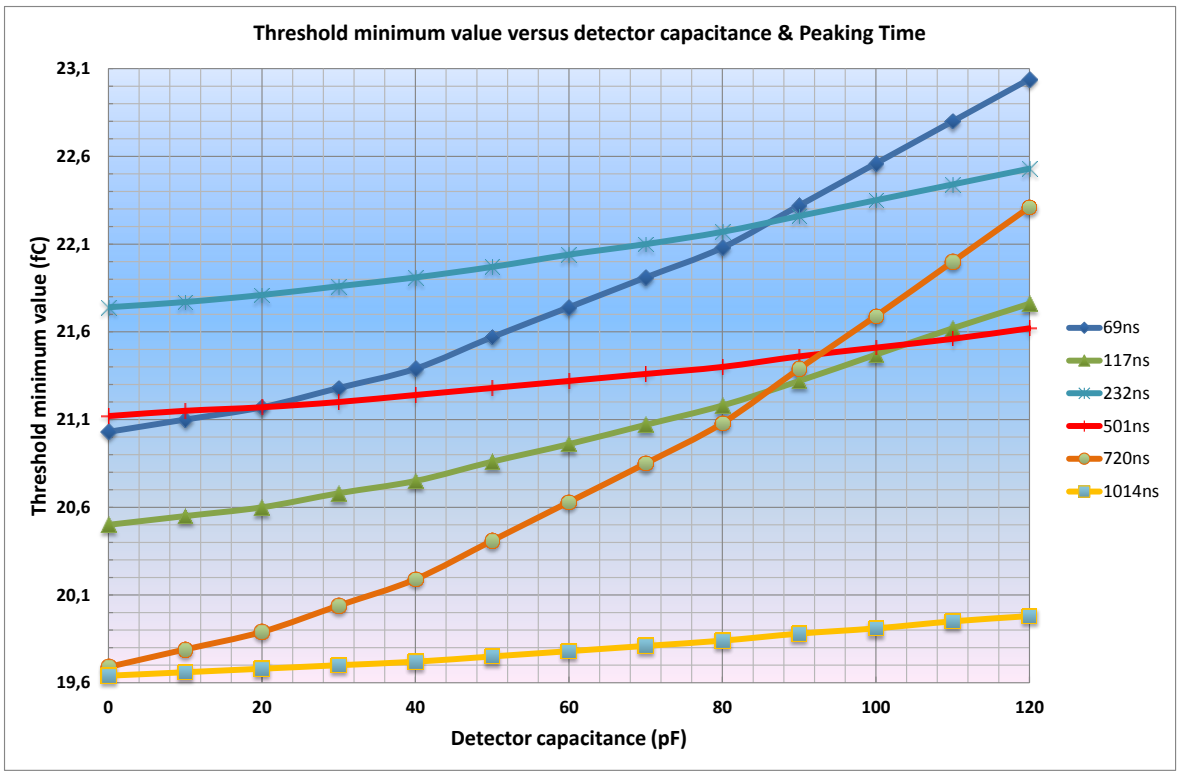


Fig. 61: Minimum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 800µA.

12.5.D Minimum threshold value at 17.5% of input dynamic range

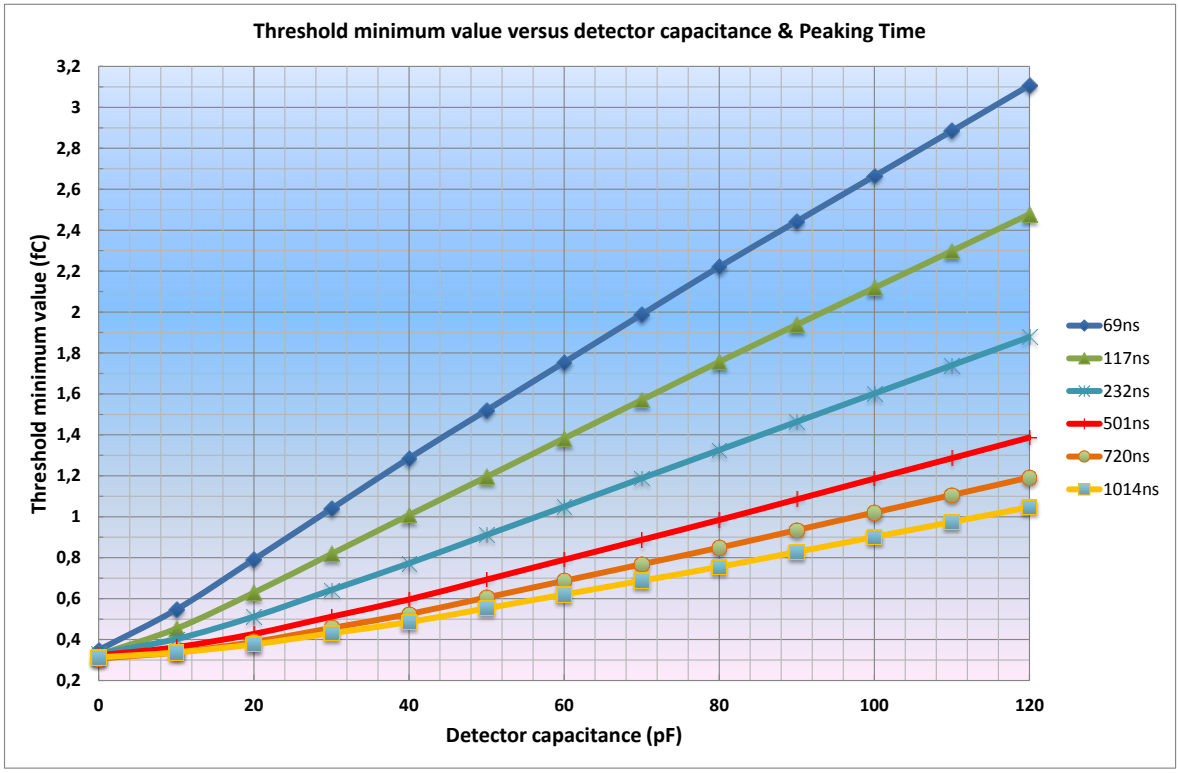


Fig. 62: Minimum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 400µA.

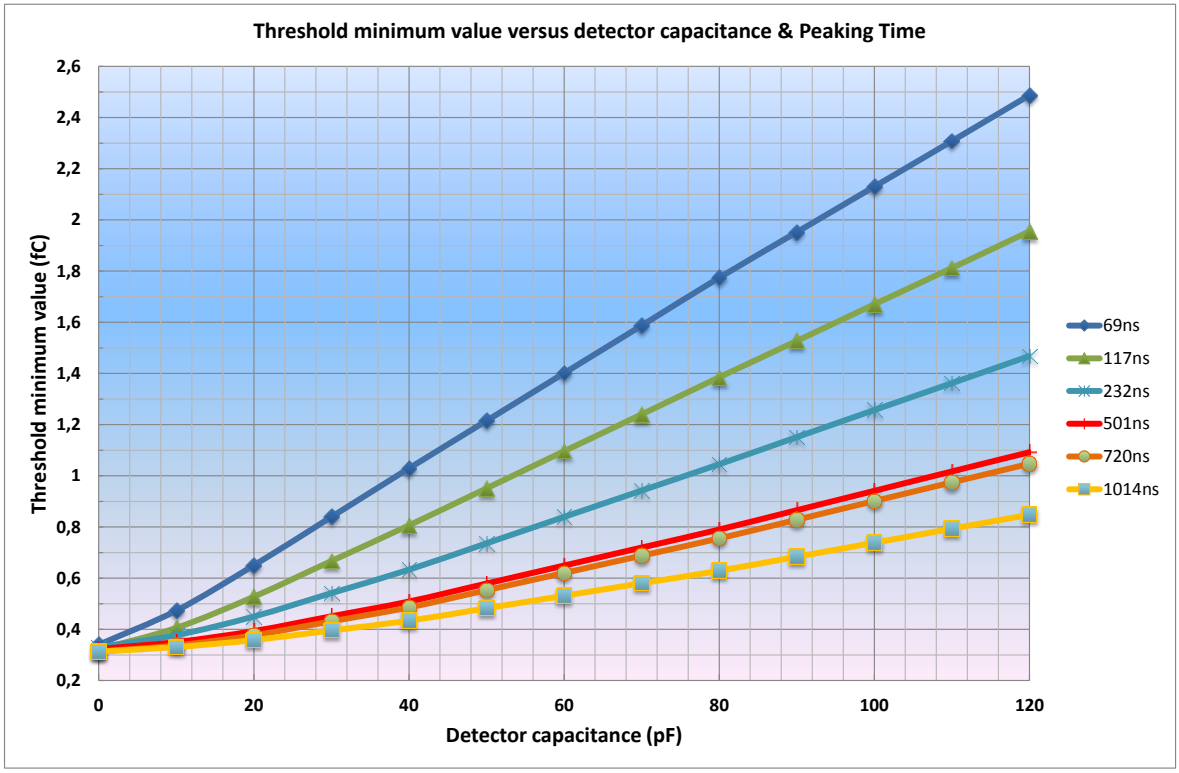


Fig. 63: Minimum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 800µA.

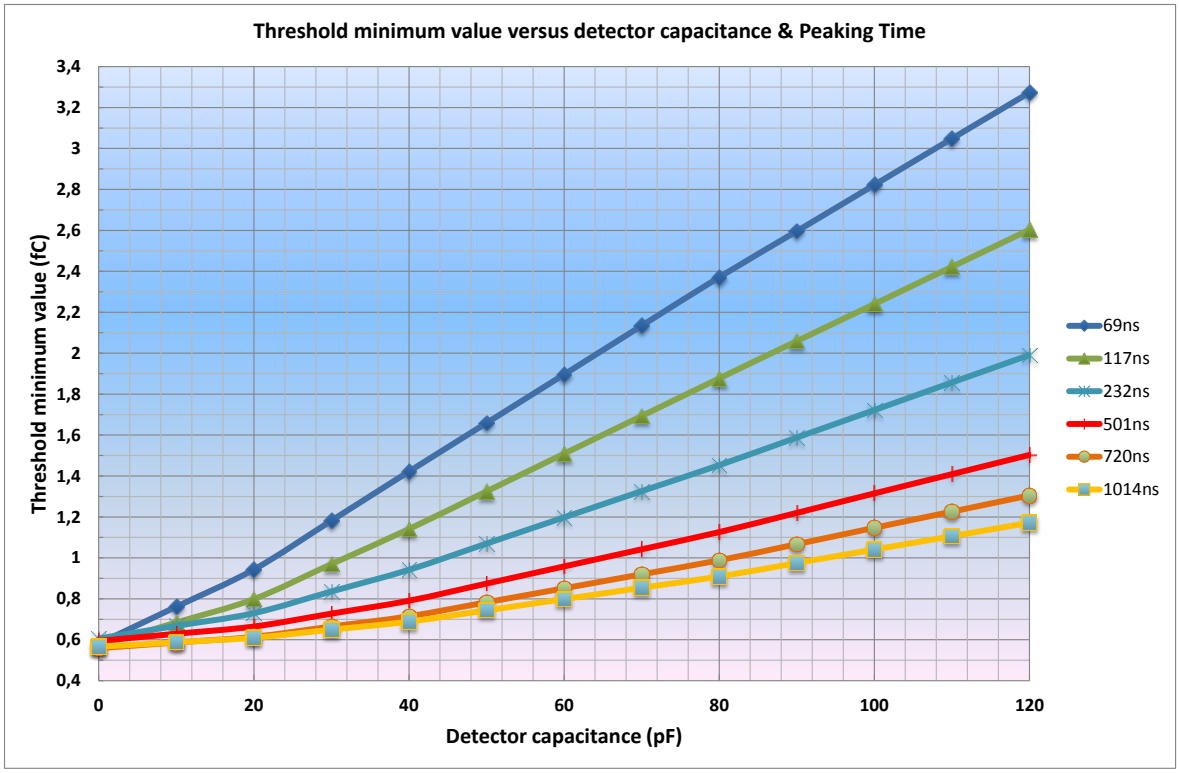


Fig. 64: Minimum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 400µA.

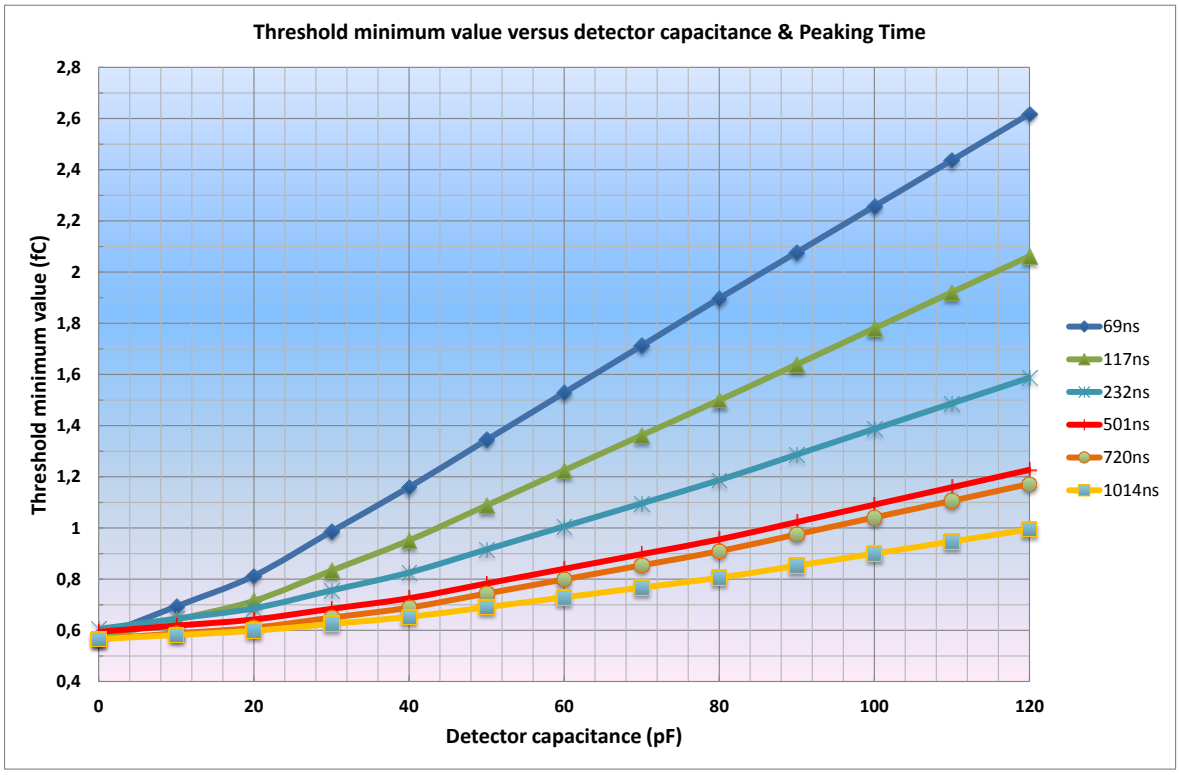


Fig. 65: Minimum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 800µA.

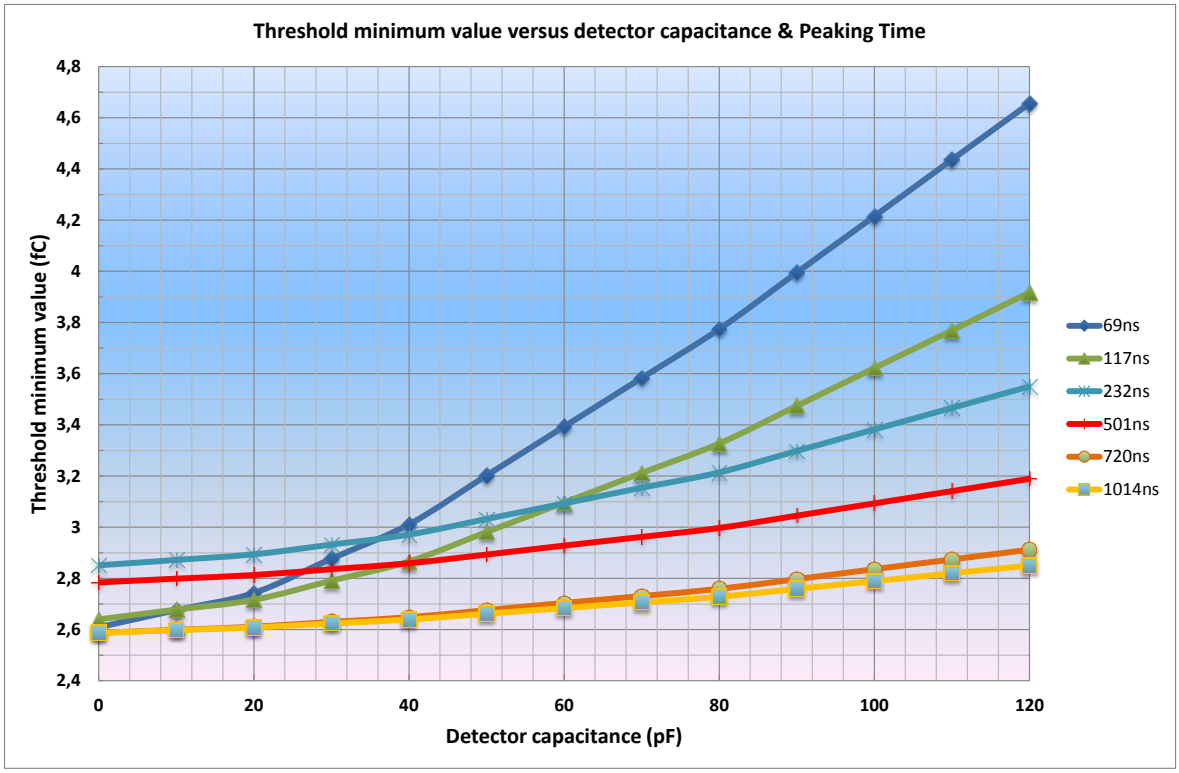


Fig. 66: Minimum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 400µA.

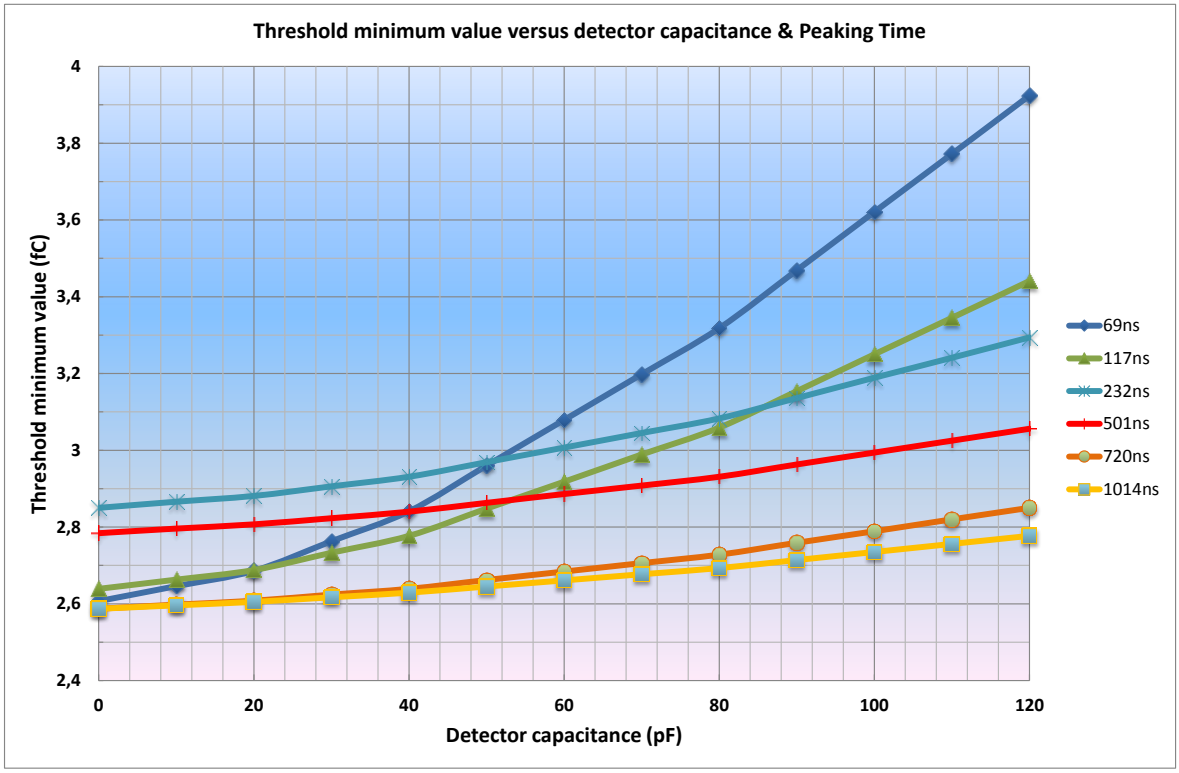


Fig. 67: Minimum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 800µA.

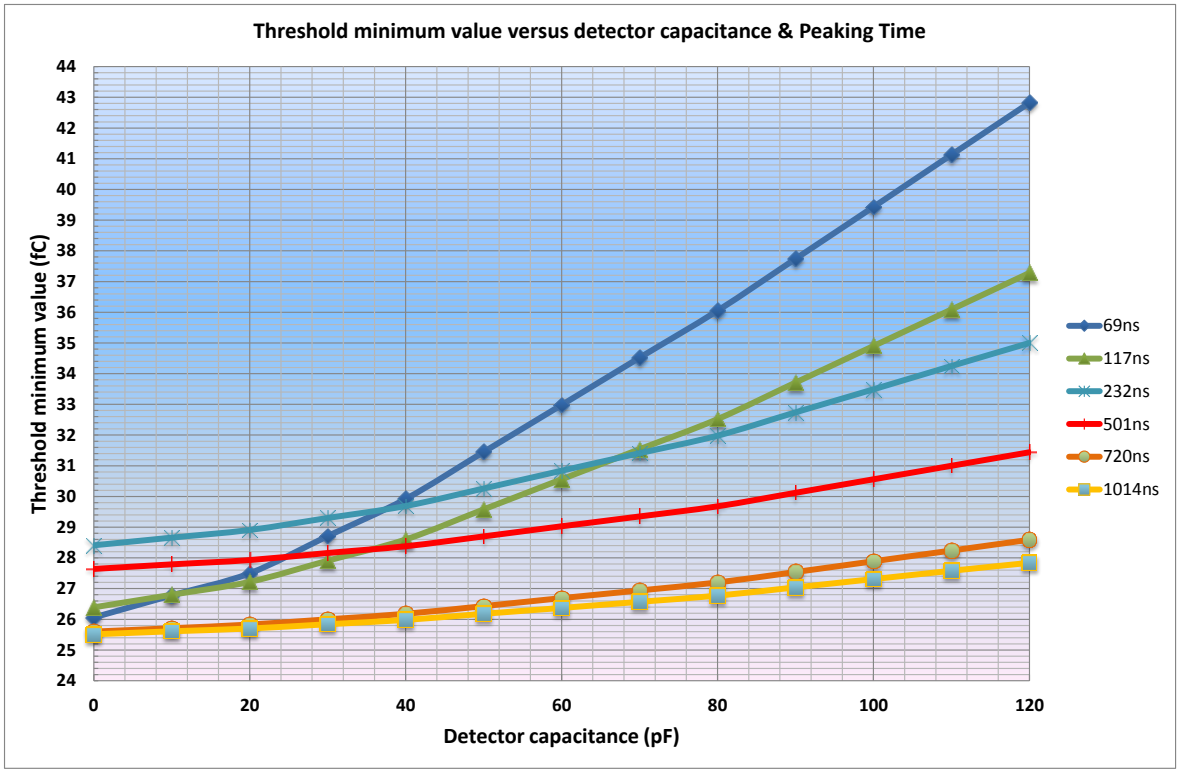


Fig. 68: Minimum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 400µA.

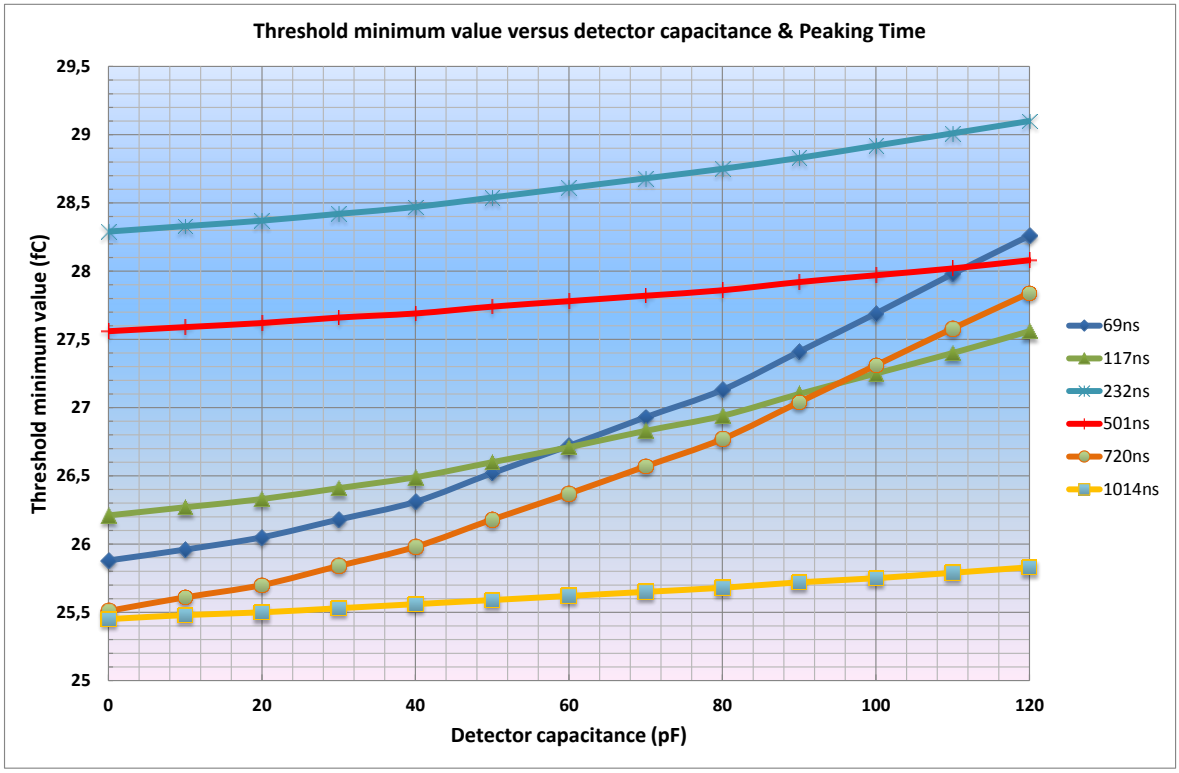


Fig. 69: Minimum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 800µA.

12.5.E Maximum threshold value at 5% of input dynamic range

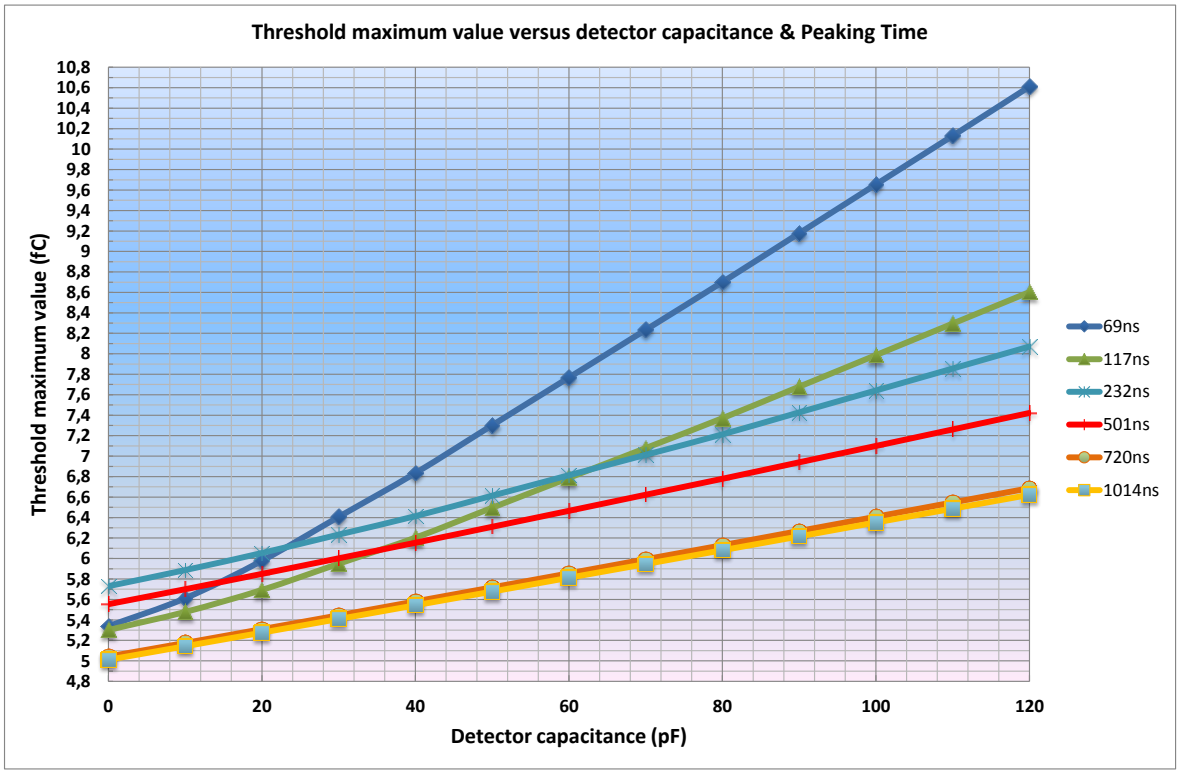


Fig. 70: Maximum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 400µA.

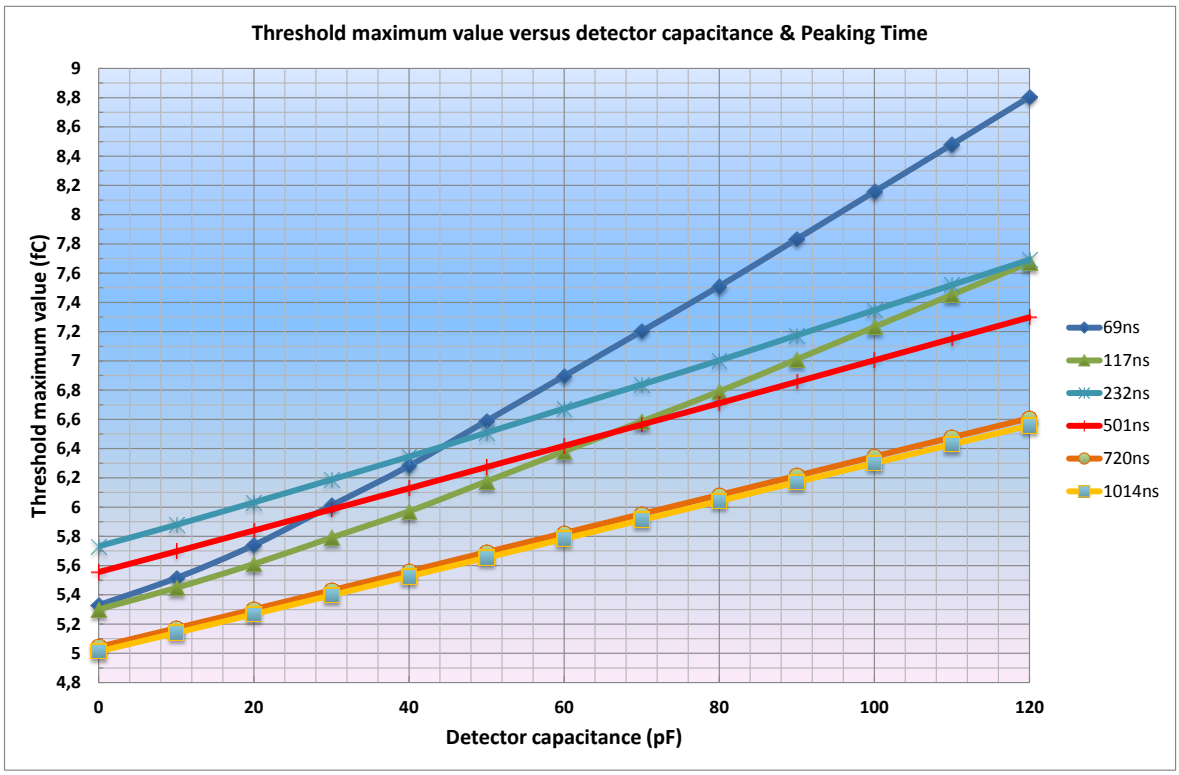


Fig. 71: Maximum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 800µA.

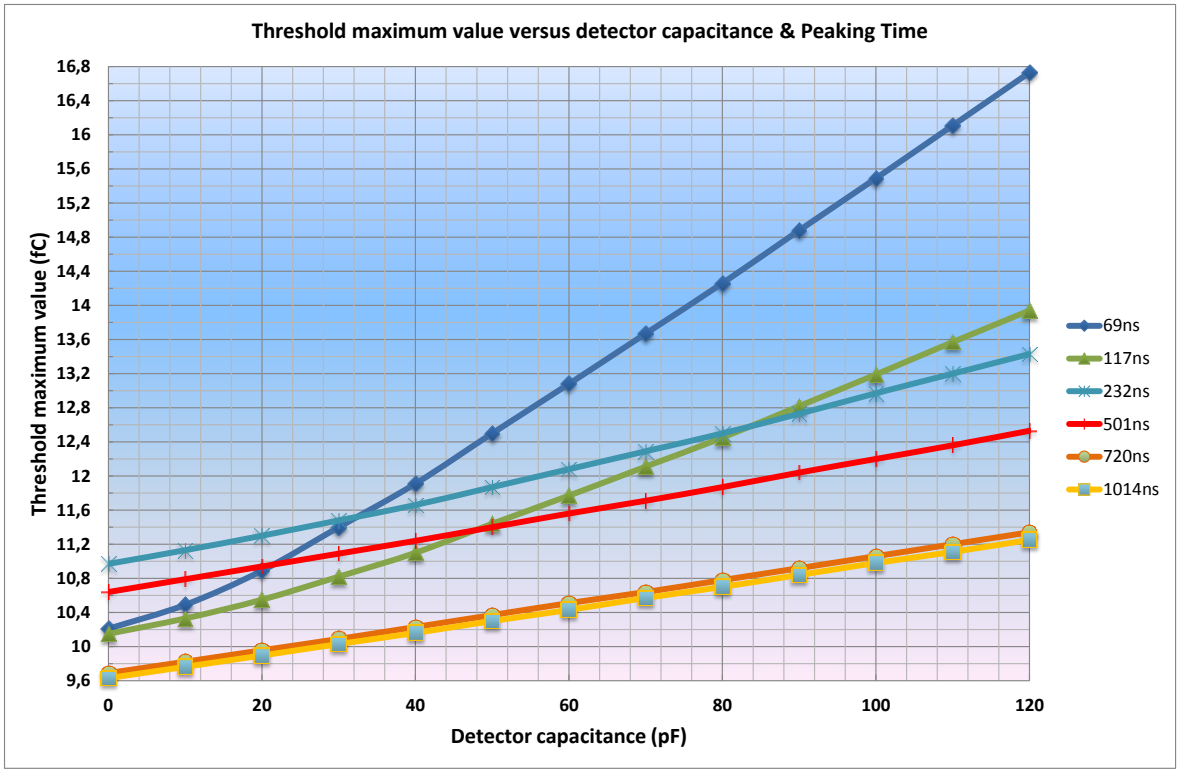


Fig. 72: Maximum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 400µA.

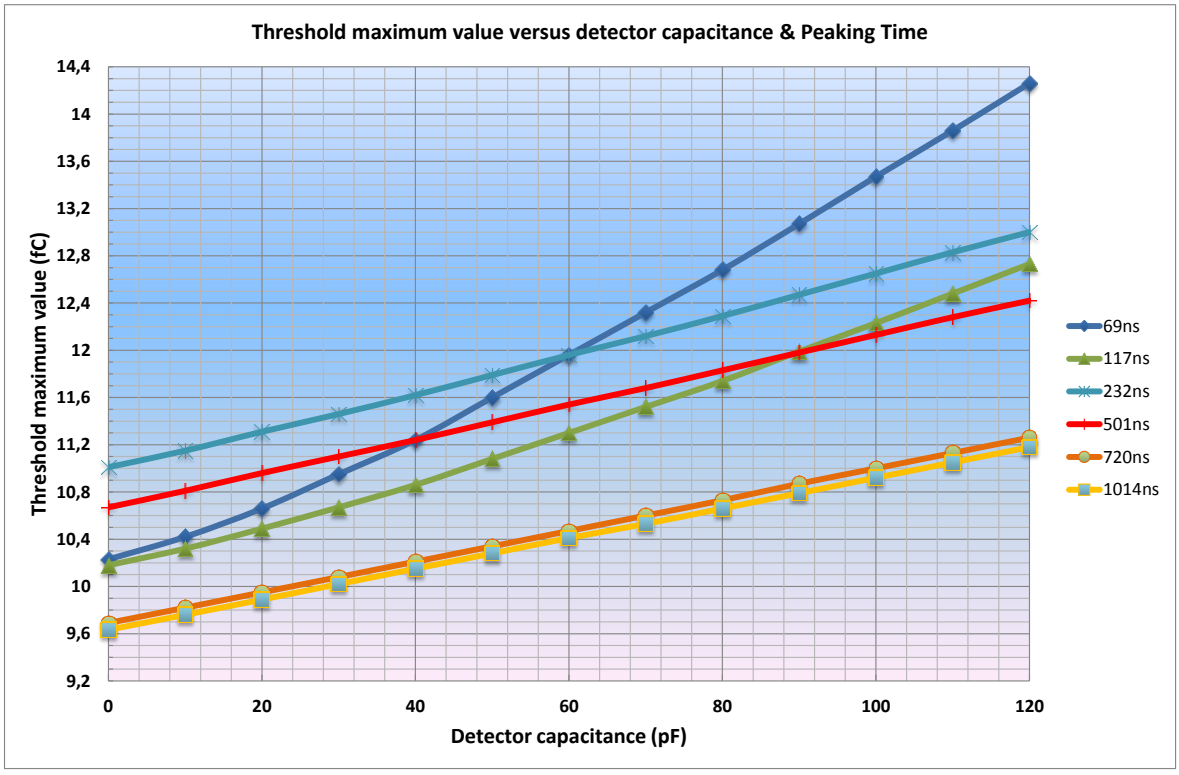


Fig. 73: Maximum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 800µA.

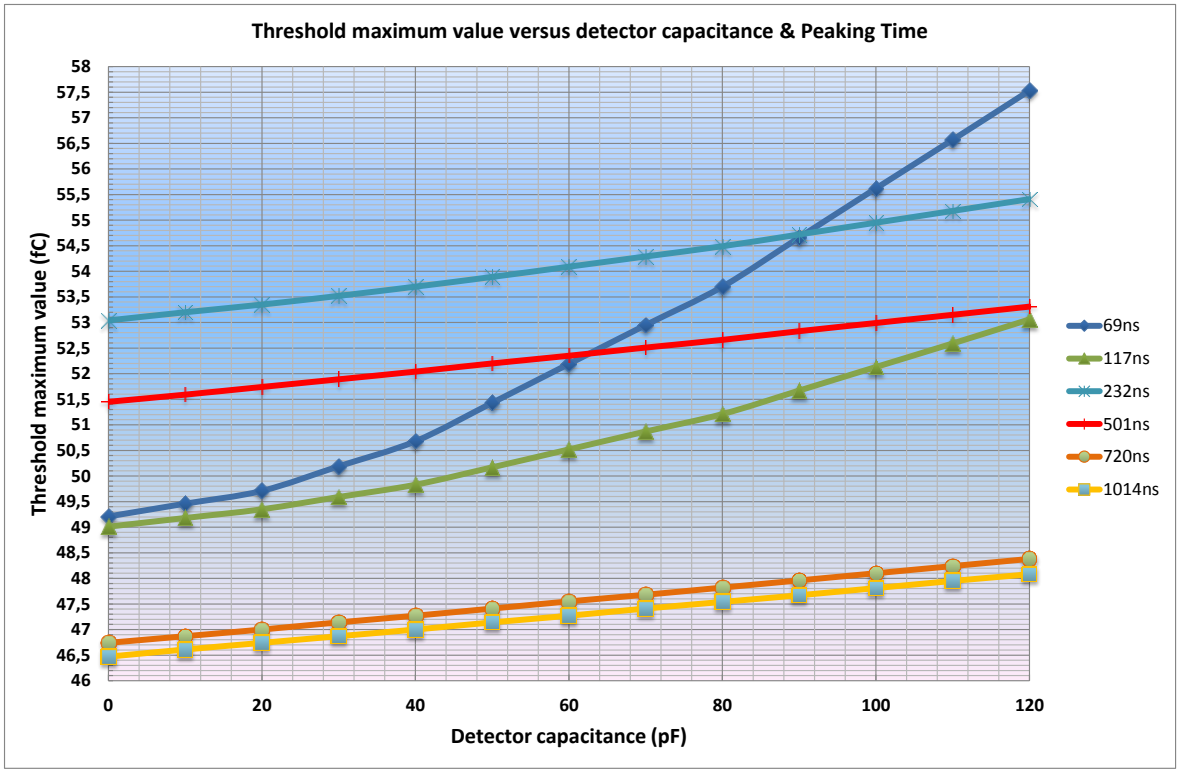


Fig. 74: Maximum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 400µA.

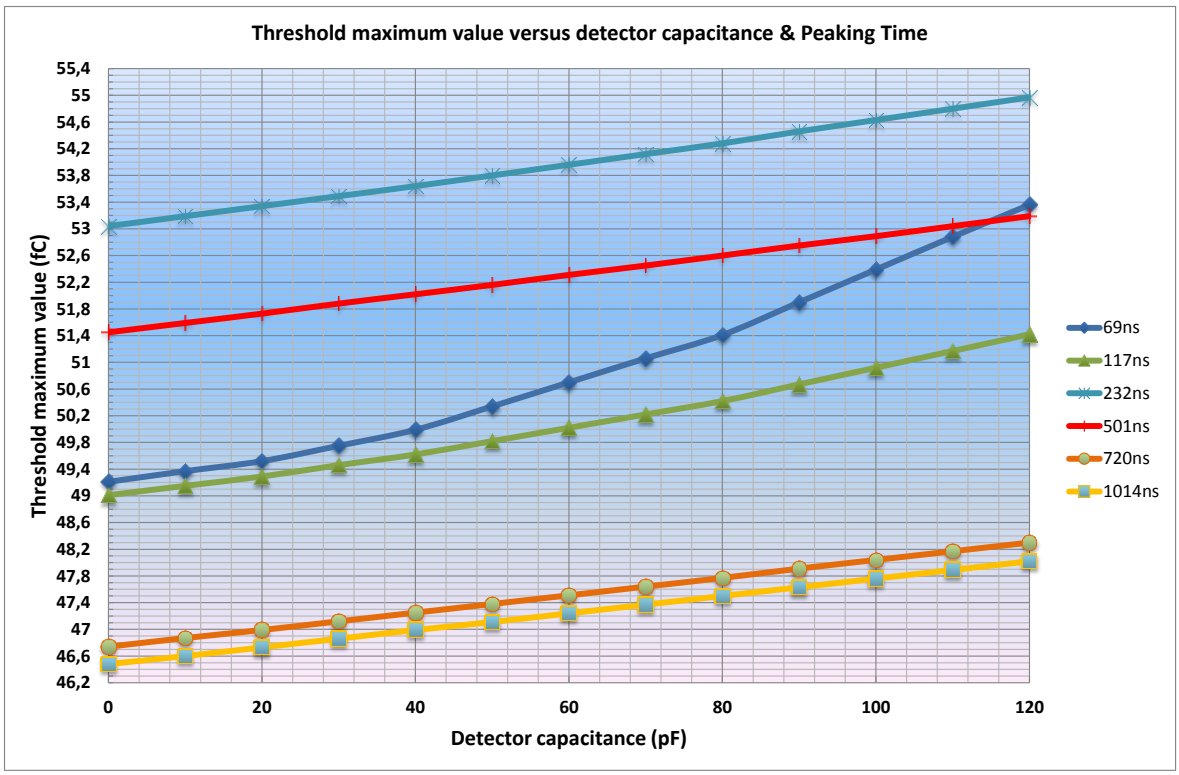


Fig. 75: Maximum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 800µA.

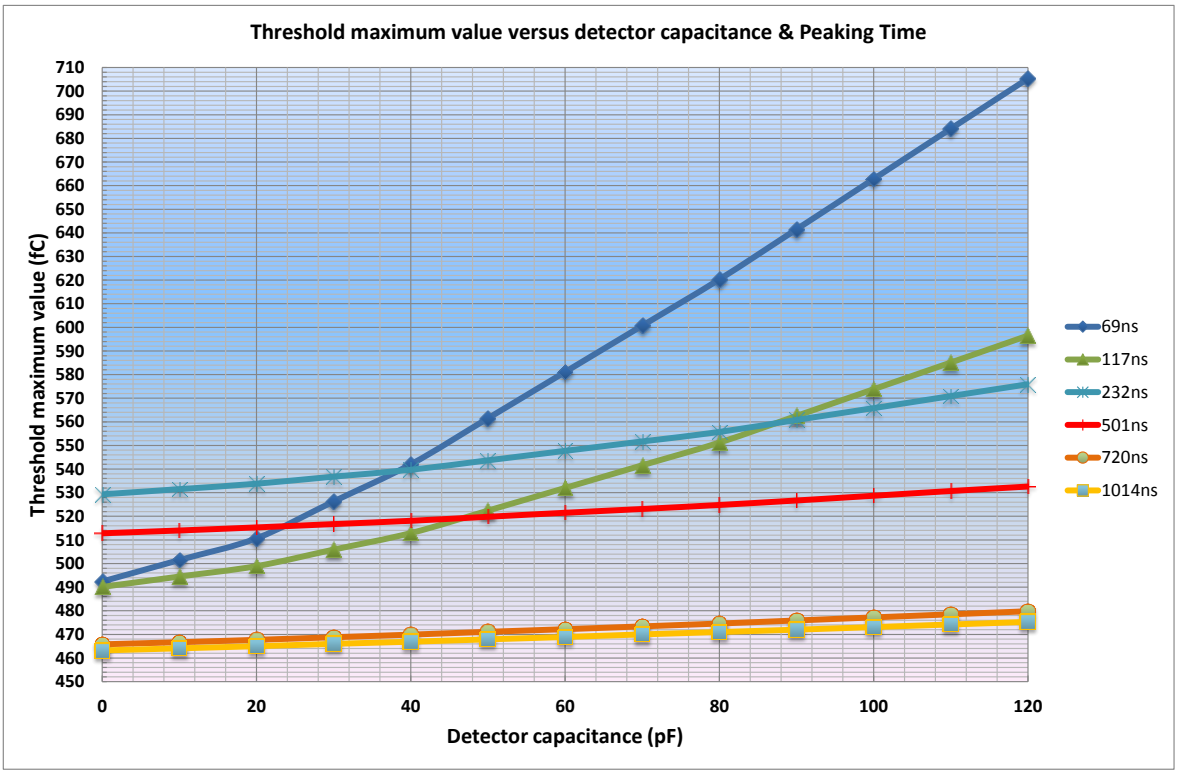


Fig. 76: Maximum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 400µA.

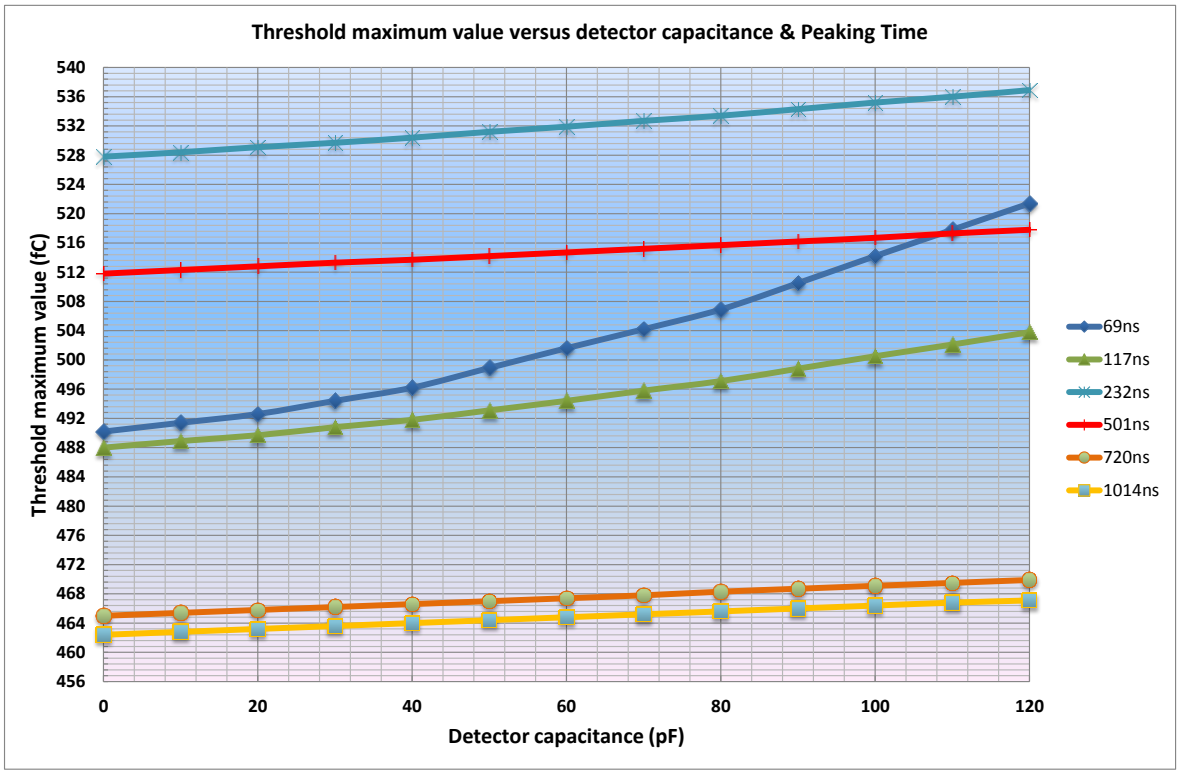


Fig. 77: Maximum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 800µA.

12.5.F Maximum threshold value at 17.5% of input dynamic range

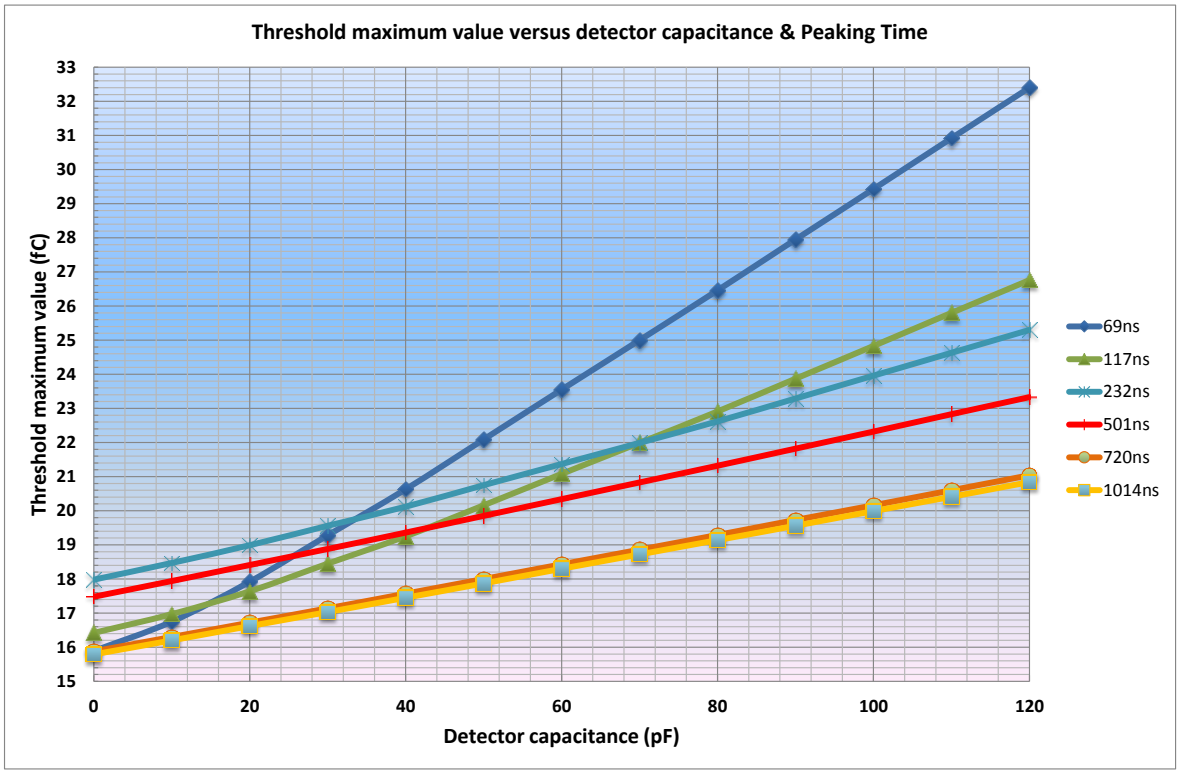


Fig. 78: Maximum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 400µA.

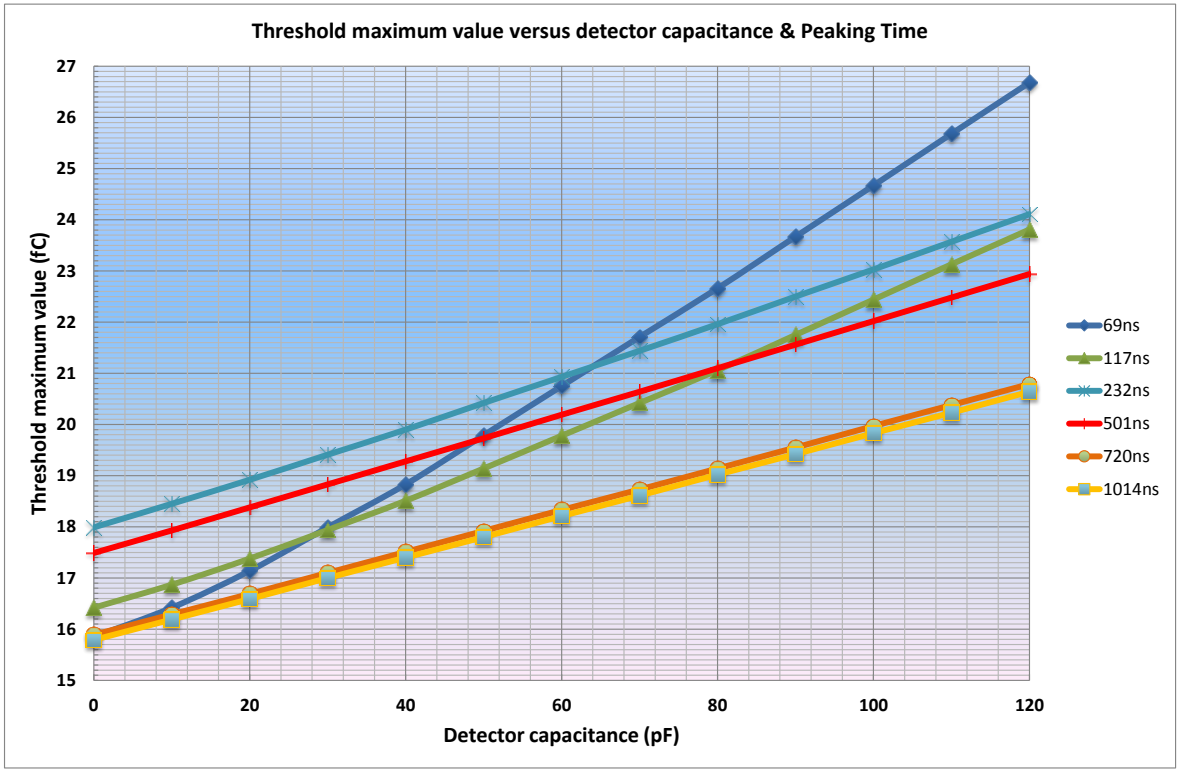


Fig. 79: Maximum threshold value vs detector capacitance for various peaking times. Range = 120 fC & I_{CSA} = 800µA.

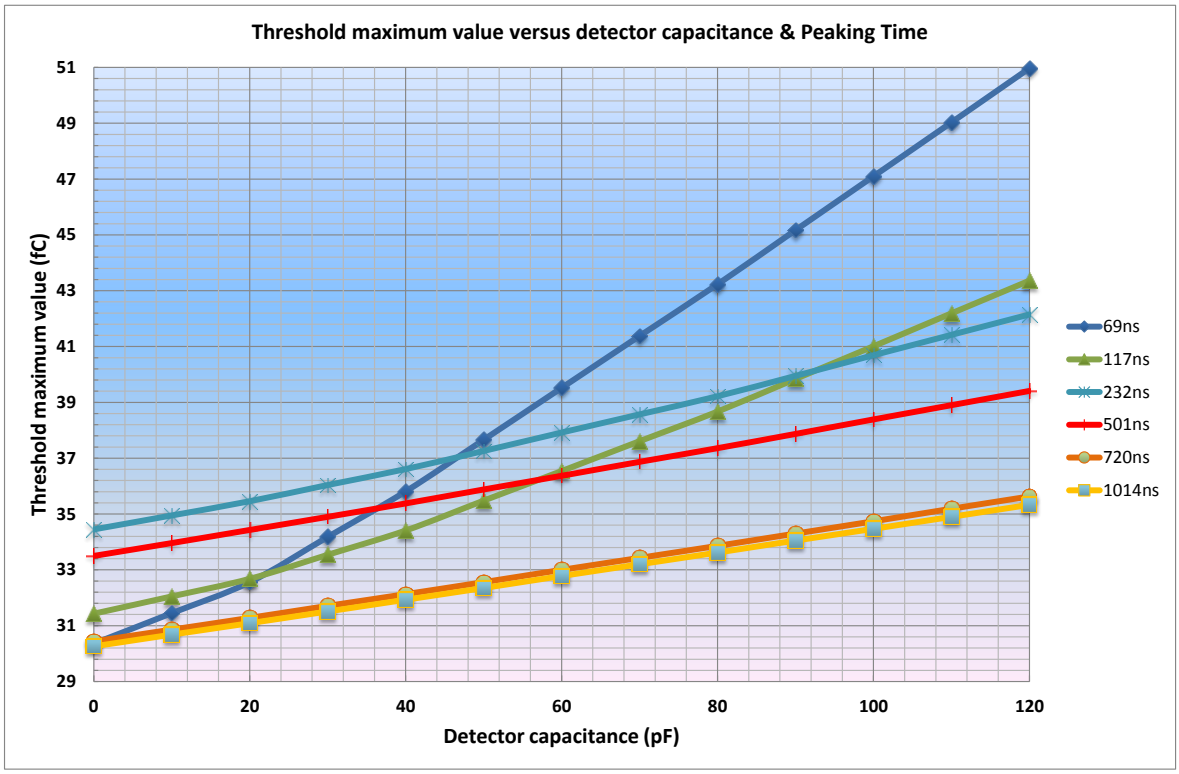


Fig. 80: Maximum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 400µA.

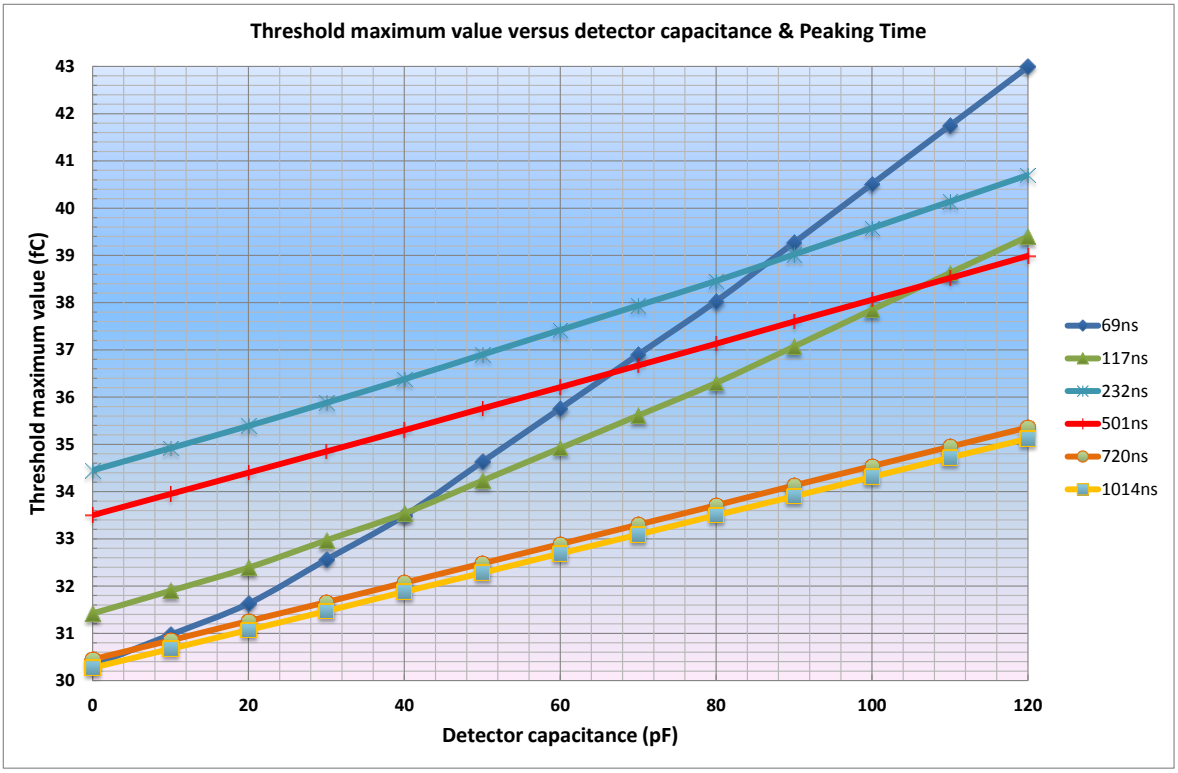


Fig. 81: Maximum threshold value vs detector capacitance for various peaking times. Range = 240 fC & I_{CSA} = 800µA.

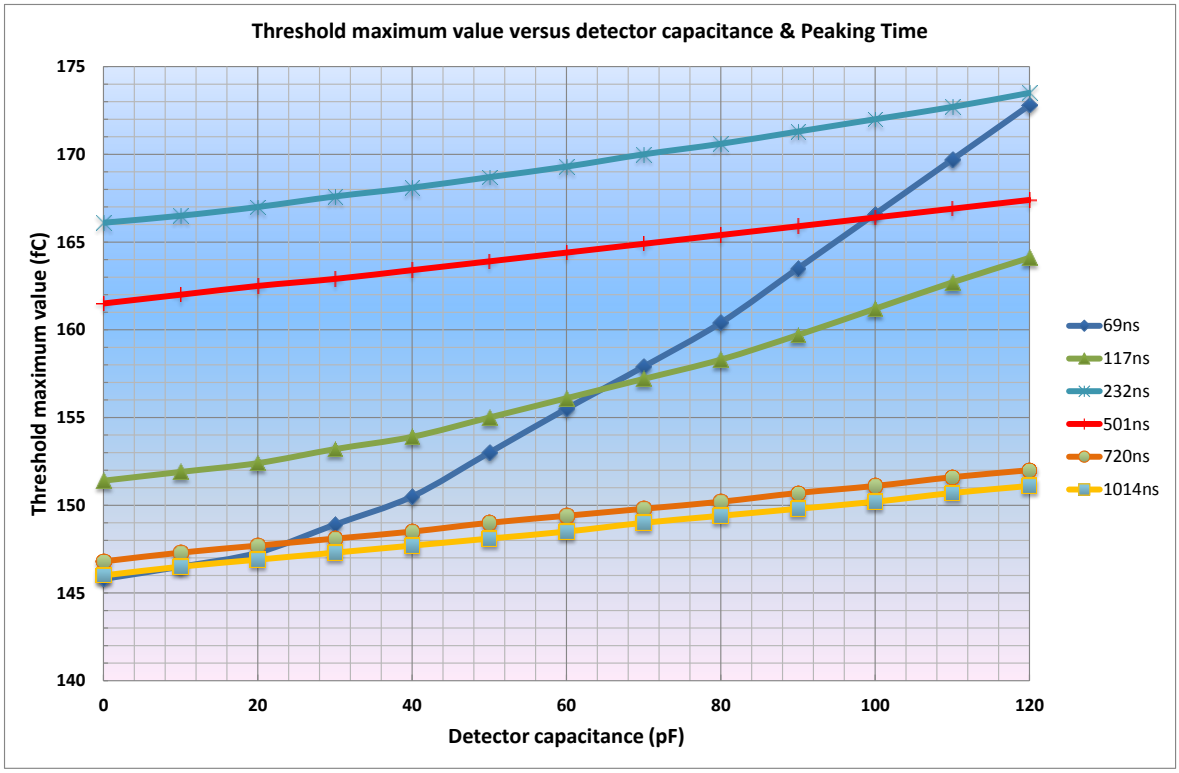


Fig. 82: Maximum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 400µA.

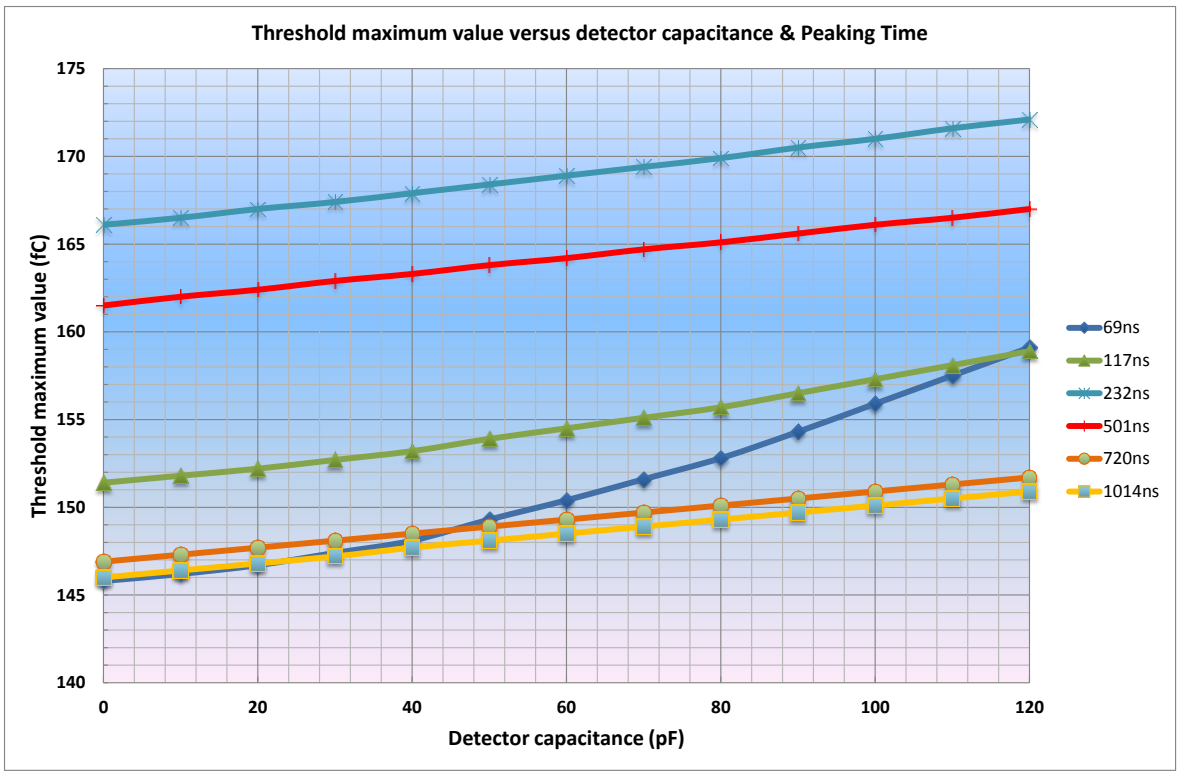


Fig. 83: Maximum threshold value vs detector capacitance for various peaking times. Range = 1 pC & I_{CSA} = 800µA.

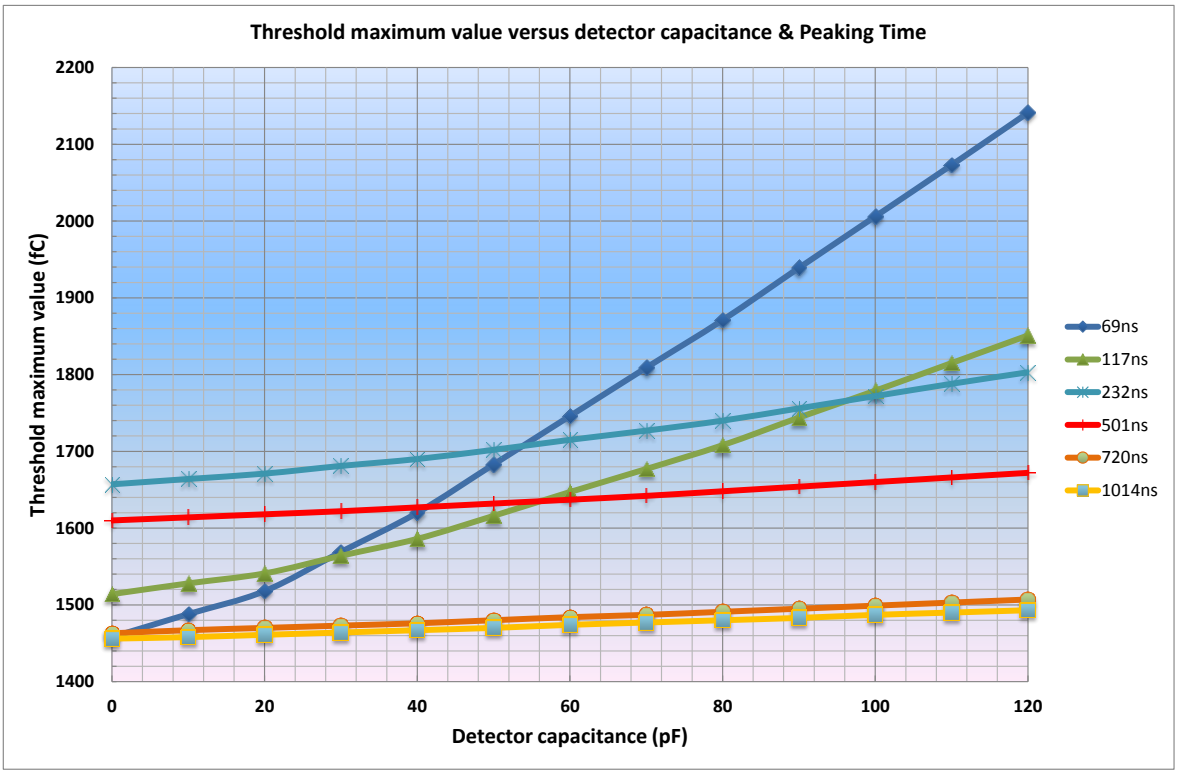


Fig. 84: Maximum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 400µA.

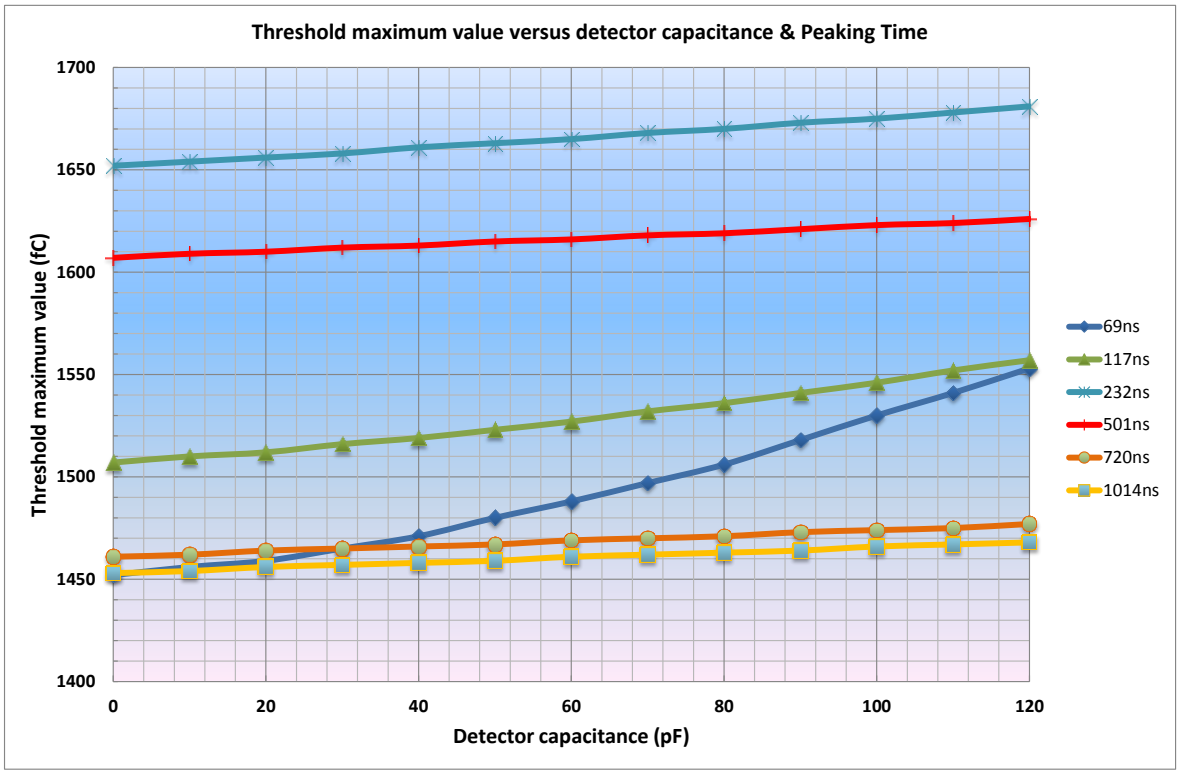


Fig. 85: Maximum threshold value vs detector capacitance for various peaking times. Range = 10 pC & I_{CSA} = 800µA.

12.6 Multiplicity transfer function

When a channel is hit, it switches its current source on a common bus of all channels, giving a Multiplicity signal. The value of elementary signal is equal to 23.244 mV (#48 ADC bins) which gives 1.482 V for the full scale (64 hit channels).

13. AGET pin configuration

The AGET chip is housed in a 160-pin Low Quad Flat Pack (LQFP-160). The package body dimensions are 28 x 28 x 1.4 mm. Its pitch is 0.65 mm with 2 mm footprint. The pin configuration is given in the **Fig. 86**.

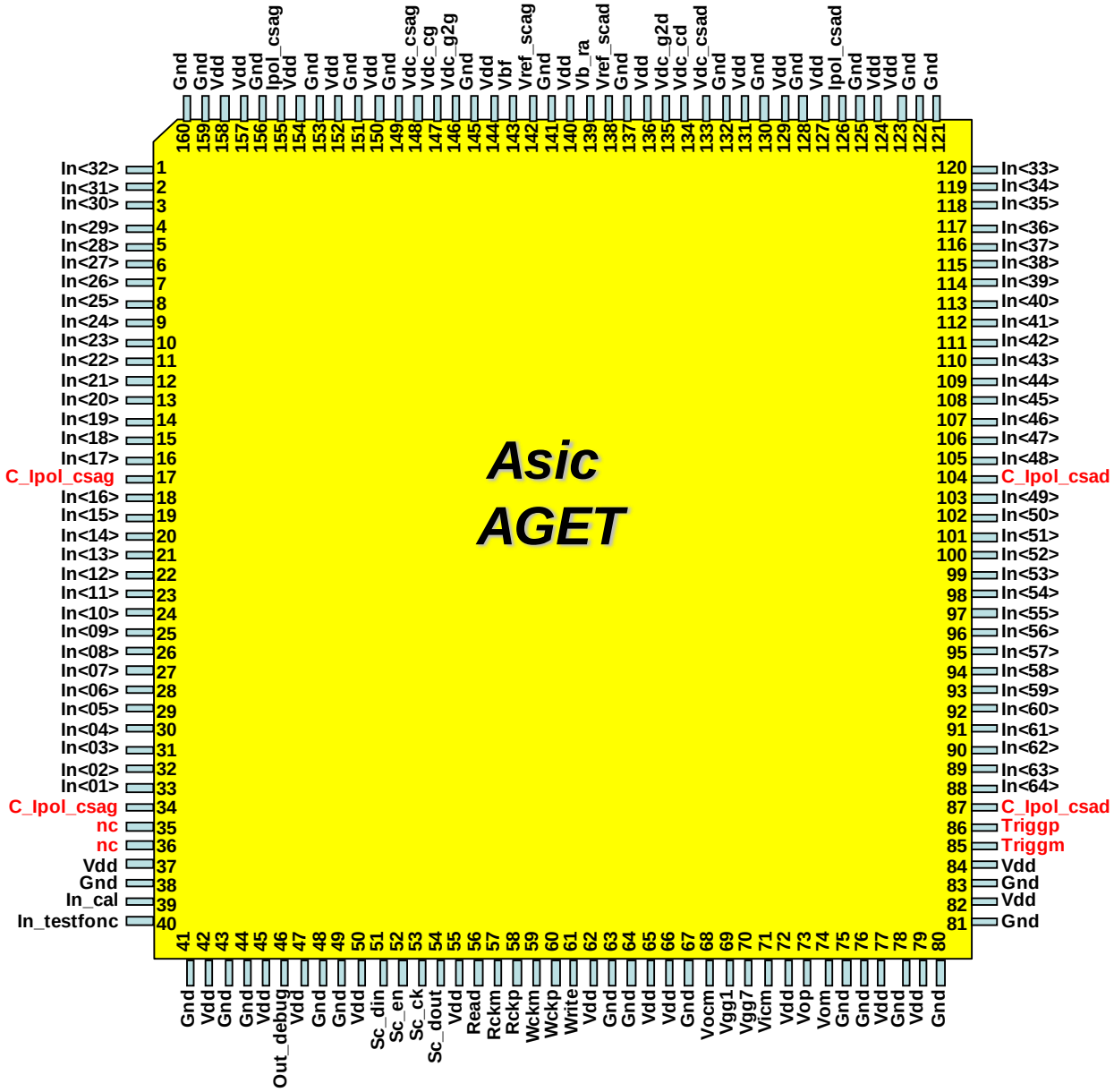


Fig. 86: The pin configuration of the AGET chip.

The description of each pin is reported in the table 43.

N° Pin	Name	Dir.	Level	Description
1 to 16	In<32> to In<17>	In	Analog	Inputs of channels 32 to 17
17	C_Ipol_csag	In	Analog	Input for internal Ipol_csag filtering
18 to 33	In<16> to In<1>	In	Analog	Inputs of channels 16 to 1
34	C_Ipol_csag	In	Analog	Input for internal Ipol_csag filtering
35 to 36	n.c.			Not connected
37	Vdd_csag	In	3.3V	Vdd for the CSA of the channels 32 to 1 & Threshold DAC
38	gnd	In	0V	Gnd for the CSA of the channels 32 to 1 & Threshold DAC
39	In_cal	In	Analog	Input for the calibration
40	In_testfonc	In	Analog	Input for the test & functionality
41	gnd	In	0V	Gnd for protection diode [37 to 84], cavity & SCA digital part guard ring.
42	Vdd_crg	In	3.3V	Vdd for the PZC of the channels 32 to 1
43	gnd	In	0V	Gnd for the PZC filter of the channels 32 to 1
44	gnd	In	0V	Gnd for the SK filter of the channels 32 to 1
45	Vdd_skg	In	3.3V	Vdd for the SK filter of the channels 32 to 1
46	Out_debug	Out	Analog	Output of the “spy” mode
47	Vdd_g2g	In	3.3V	Vdd for the Gain -2 of the channels 32 to 1 & 2 FPN channels; Threshold gain & LEAD input stage.
48	gnd	In	0V	Gnd for the Gain -2 of the channels 32 to 1 & 2 FPN channels; Threshold gain & LEAD input stage.
49	gnd	In	0V	Gnd return buffer + Matrix
50	vdd	In	3.3V	Vdd return buffer + Matrix
51	Sc_din	In	CMOS 3.3V	Serial data input of Slow Control / Hit channel registers
52	Sc_en	In	CMOS 3.3V	Chip Select input of Slow Control / Hit channel registers
53	Sc_ck	In	CMOS 3.3V	Serial clock input of Slow Control / Hit channel registers
54	Sc_dout	Out	CMOS 3.3V	Serial data output of Slow Control / Hit channel registers
55	Vdd_prob	In	3.3V	Vdd for protection diode [37 to 84], SCA digital part guard ring.
56	read	In	CMOS 3.3V	SCA read mode
57	rckm	In	LVDS	SCA Negative read clock
58	rckp	In	LVDS	SCA Positive read clock
59	wckm	In	LVDS	SCA Negative write clock
60	wckp	In	LVDS	SCA Positive write clock
61	write	In	CMOS 3.3V	SCA write mode
62	vdd	In	3.3V	Vdd LVDS receiver & block SCA Write Clock
63	gnd	In	0V	Gnd LVDS receiver & block SCA Write Clock
64	gnd	In	0V	Gnd SCA logic; Slow & hit register Control; Trigger
65	vdd	In	3.3V	Vdd SCA logic; Slow & hit register Control; Trigger
66	vdd	In	3.3V	Vdd SCA Readout Amplifier + Matrix
67	gnd	In	0V	Gnd SCA Readout Amplifier + Matrix
68	vocm	In	VddADC/2	Common mode output voltage of the Readout buffer
69	Vgg1	Out	Current 2mA	Current bias of the input stage of Readout buffer
70	Vgg7	Out	Current 1mA	Current bias of the output stage of Readout buffer
71	vicm	In	1.45V mean	Common mode input voltage of the Readout buffer
72	Vdd_out	In	3.3V	Vdd of the Readout buffer & SCA buffer
73	vop	Out	Analog	Positive output of the Readout buffer
74	vom	Out	Analog	Negative output of the Readout buffer
75	gnd	In	0V	Gnd buffer out + logic
76	gnd	In	0V	Gnd for the Gain -2 of the channels 33 to 64 & 2 FPN channels; Threshold gain & LEAD input stage.
77	Vdd_g2d	In	3.3V	Vdd for the Gain -2 of the channels 33 to 64 & 2 FPN channels; Threshold gain & LEAD input stage.
78	gnd	In	0V	Gnd for the SK filter of the channels 33 to 64
79	Vdd_skd	In	3.3V	Vdd for the SK filter of the channels 33 to 64
80	gnd	In	0V	Gnd for cavity

N° Pin	Name	Dir.	Level	Description
81	gnd	In	0V	Gnd for the PZC filter of the channels 33 to 64
82	Vdd_crd	In	3.3V	Vdd for the PZC filter of the channels 33 to 64
83	gnd	In	0V	Gnd for the CSA of the channels 33 to 64 & Threshold DAC
84	Vdd_csad	In	3.3V	Vdd for the CSA of the channels 33 to 64 & Threshold DAC
85	Triggm	Out	LVDS	Trigger negative output
86	Triggp	Out	LVDS	Trigger positive output
87	C_Ipol_csad	In	Analog	Input for internal Ipol_csad filtering
88 to 103	In<64> to In<49>	In	Analog	Inputs of channels 64 to 49
104	C_Ipol_csad	In	Analog	Input for internal Ipol_csad filtering
105 to 120	In<48> to In<33>	In	Analog	Inputs of channels 48 to 33
121	gnd	In	0V	Gnd for cavity
122	gnd	In	0V	Gnd for protection diode [33 to 64]
123	Vdd_proind	In	3.3V	Vdd for protection diode [33 to 64]
124	Vdd_csad	In	3.3V	Vdd for the CSA of the channels 33 to 64 & Threshold DAC
125	gnd	In	0V	Gnd for the CSA of the channels 33 to 64 & Threshold DAC
126	Ipol_csad	Out	Current	Current supply of the input transistors of CSA [33 to 64]
127	Vdd_crd	In	3.3V	Vdd for the PZC of the channels 33 to 64
128	gnd	In	0V	Gnd for the PZC of the channels 33 to 64
129	Vdd_skd	In	3.3V	Vdd for the SK filter of the channels 33 to 64
130	gnd	In	0V	Gnd for the SK filter of the channels 33 to 64
131	Vdd_g2d	In	3.3V	Vdd for the Gain -2 of the channels 33 to 64 & 2 FPN channels; Threshold gain & LEAD input stage.
132	gnd	In	0V	Gnd for the Gain -2 of the channels 33 to 64 & 2 FPN channels; Threshold gain & LEAD input stage.
133	Vdc_csad	In	1.8V [2.8V]	DC output level voltage of the CSA [33 to 64]
134	Vdc_cd	In	2.2V [0.7V]	DC output level voltage of the PZC & SK filter [33 to 64]
135	Vdc_g2d	In	0.7V [2.2V]	DC output level voltage of the Gain -2 [33 to 64 & 2 FPN channels]
136	Vdd	In	3.3V	Vdd SCA Readout Amplifier + Matrix
137	gnd	In	0V	Gnd SCA Readout Amplifier + Matrix
138	vref_scad	In	0.7V	DC reference level voltage of the SCA
139	vb_ra	in/out	analog	Current source voltage of the internal readout buffer; Control purpose
140	vdd_proh	In	3.3V	Vdd for protection diode [124 to 157]
141	gnd	In	0V	Gnd for protection diode [124 to 157]
142	vref_scag	In	0.7V	DC reference level voltage of the SCA
143	vbf	in/out	analog	Current source voltage of the Matrix return bus
144	Vdd	In	3.3V	Vdd return buffer + Matrix
145	gnd	In	0V	Gnd return buffer + Matrix
146	Vdc_g2g	In	0.7V [2.2V]	DC output level voltage of the Gain -2 [32 to 1 & 2 FPN channels]
147	Vdc_cg	In	2.2V [0.7V]	DC output level voltage of the PZC & SK filter [32 to 1]
148	Vdc_csag	In	1.8V [2.8V]	DC output level voltage of the CSA [32 to 1]
149	gnd	In	0V	Gnd for the Gain -2 of the channels 32 to 1 & 2 FPN channels; Threshold gain & LEAD input stage.
150	Vdd_g2g	In	3.3V	Vdd for the Gain -2 of the channels 32 to 1 & 2 FPN channels; Threshold gain & LEAD input stage.
151	gnd	In	0V	Gnd for the SK filter of the channels 32 to 1
152	Vdd_skg	In	3.3V	Vdd for the SK filter of the channels 32 to 1
153	gnd	In	0V	Gnd for the PZC of the channels 32 to 1
154	Vdd_crg	In	3.3V	Vdd for the PZC filter of the channels 32 to 1
155	Ipol_csag	in/out	Current	Current supply of the input transistors of CSA [32 to 1]
156	gnd	In	0V	Gnd for the CSA of the channels 32 to 1 & Threshold DAC
157	Vdd_csag	In	3.3V	Vdd for the CSA of the channels 32 to 1 & Threshold DAC
158	Vdd_proing	In	3.3V	Vdd for protection diode [32 to 1]
159	gnd	In	0V	Gnd for protection diode [32 to 1]
160	gnd	In	0V	Gnd for cavity

Table 43: Pin function descriptions of AGET chip.

14. The AGET layout

The view of the AGET chip layout is given in the **Fig. 87**. The circuit is manufactured using the AMS CMOS 0.35µm technology. The die area is 8557.1 µm (+240µm) x 7630.8 µm (+240 µm).

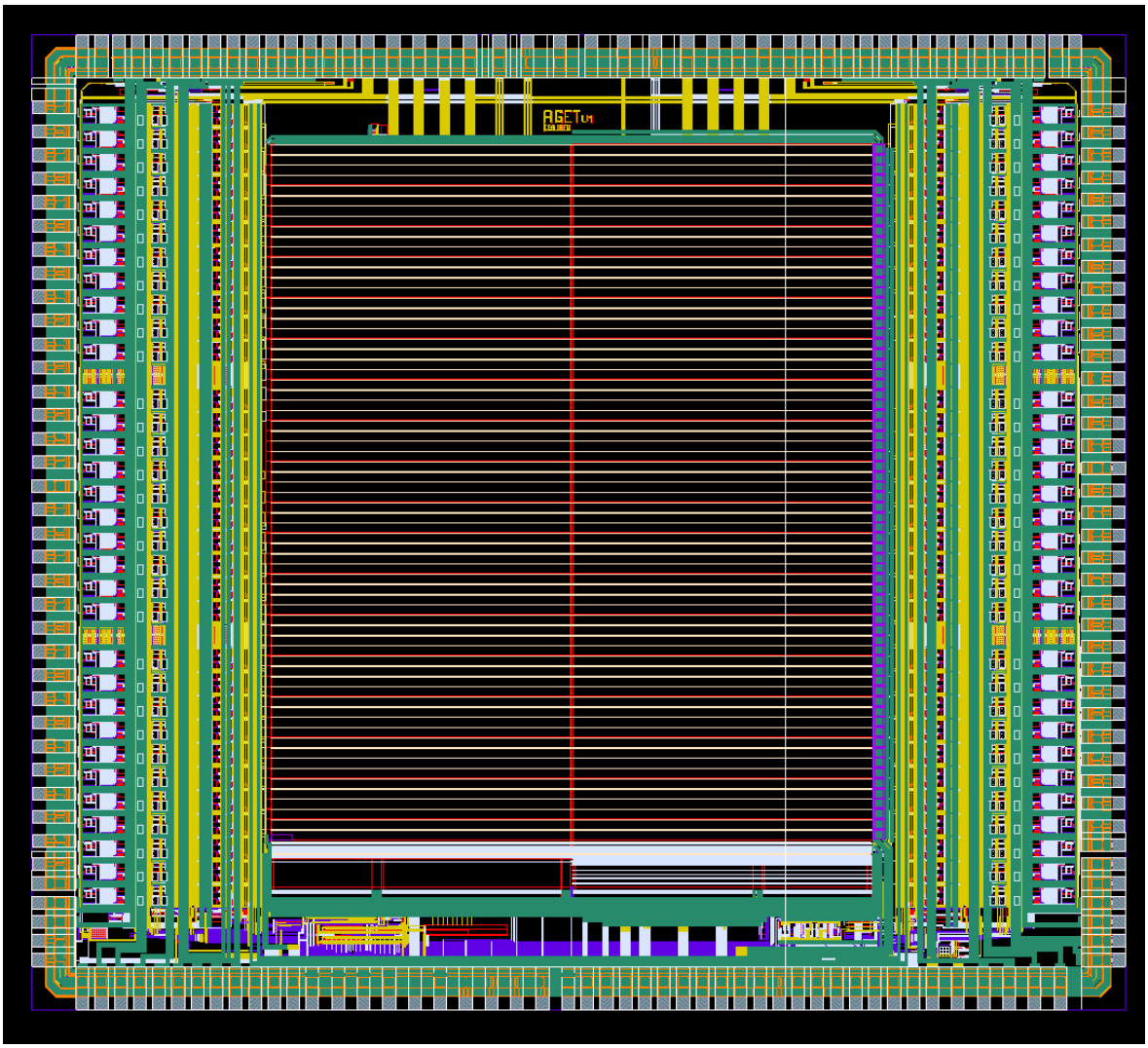


Fig. 87: Layout of the AGET chip.

The number of components is around 700 000 (# 650 000 transistors; # 40 000 capacitors; # 5000 resistors).

15. Synthesis of final AGET requirements

The final specifications of the AGET in the production version are summarized in the table 44.

Parameter	Value
Polarity of detector signal	Negative or Positive
Channels number	64
External Preamplifier	Yes; access to the filter or SCA input (external CSA)
Charge measurement	
Input dynamic range	120 fC, 240 fC, 1 pC, 10 pC
Gain	Adjustable per channel
Output dynamic range	2V p-p (differential)
I.N.L	< 2%
Resolution	< 850 e- (Gain: 120fC; Peaking Time: 200ns; Cinput < 30pF)
Sampling	
Peaking time	50 ns to 1 µs (16 values)
SCA time bin number	512 or 2 x 256 cells
Sampling Frequency	1 MHz to 100 MHz
Multiplicity	
Multiplicity signal	Analog “OR” of 64 discriminator outputs
Input dynamic range	5% or 17.5% of input channel input charge range
I.N.L	< 5%
Threshold value	7-bit DAC [(3-bit + polarity bit) common DAC + 4-bit DAC/channel]
Readout	
Readout frequency	25 MHz
Channel Readout mode	Hit, selected or all
SCA Readout mode	1 to 512 cells
Test	
calibration	1 channel among 64; 1 external test capacitor
test	1 channel among 64; internal test capacitor (1 among 4)
functional	1 to 64(68) channels; 1 internal test capacitor per channel
Counting rate	< 1 kHz
Power consumption	< 10 mW / channel @ 3.3V

Table 44: Synthesis of AGET chip.

Annexe 1: List of modification

Few modifications have been made on the production version of AGET circuit. This is the list of them.

A/ The input serial resistor of 10 Ohms at the input of the channel is removed since it cannot protect the input against TPC sparks and it generates additional noise.

B/ The unity value of multiplicity signal can be adjusted by the 2-bit slow control state1<28:29> according to the process corners. These 2-bit are also used to control the width of the multiplicity signal.

C/ The input dynamic range of the discriminator can be fixed to 5% or 17.5% of the input dynamic range of the analog channel. The slow control bit state2<24> permits to define this gain.

D/ The version number of the production version is set to: 0x0202 (0x0201 for previous version).

Annexe 2: Package description

The description of the package is presented in the **Fig. 88** & **Fig. 89**.

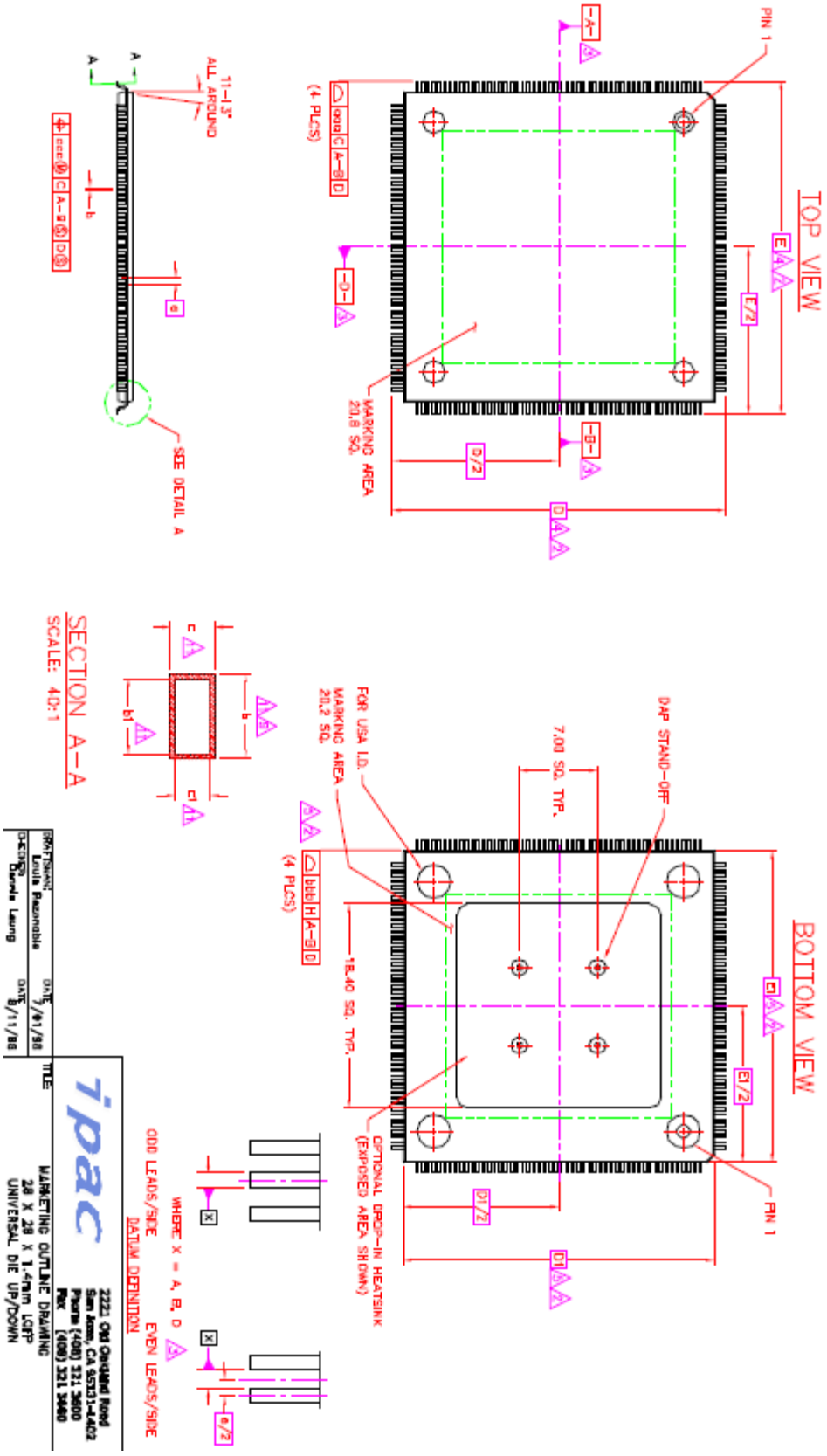
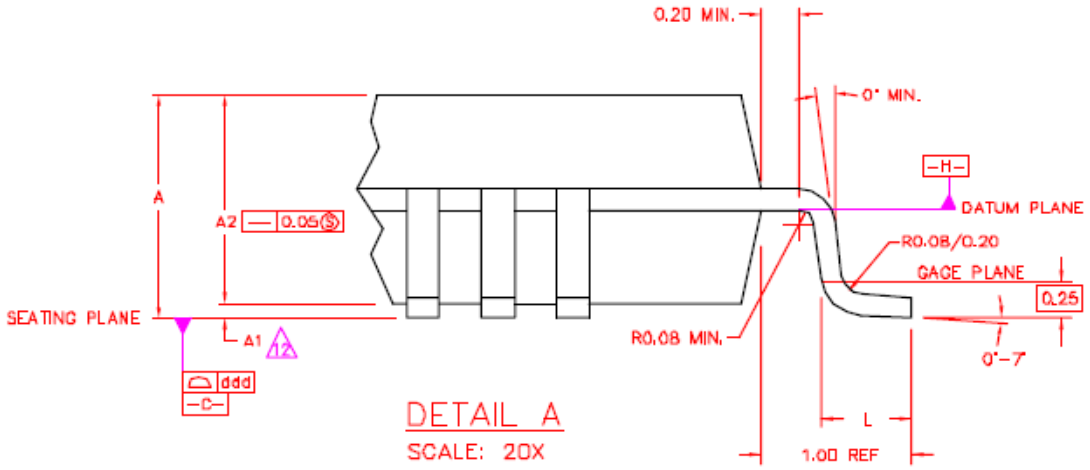


Fig. 88: Package description.



SYMBOL	LEAD COUNT; FOOT PRINT 160; 2.0 FP			NOTE
	MIN.	NOM.	MAX.	
A	---	---	1.60	
A1	0.05	---	0.15	
A2	1.35	1.40	1.45	
D	30.00 BSC			
D1	28.00 BSC			
E	30.00 BSC			
E1	28.00 BSC			
L	0.45	0.60	0.75	
e	0.65 BSC			
b	0.22	===	0.38	
b1	0.22	0.28	0.33	
c	0.09	===	0.20	
c1	0.09	---	0.16	
	Tolerances of form and position			
aaa	0.20			
bbb	0.20			
ccc	0.12			
ddd	0.08			

Fig. 89: Package dimension.

Annexe 3: Bonding Diagram

The 171 pads of the chip are more than the available 160 pads of the package (LQFP-160 pins) selected. Therefore double or triple bonding is enforced. The reason of this is to reduce the inductance effect of the bonding for the digital supply (SCA & Trigger). The bonding diagram of AGET is reported in the **Fig. 90**.

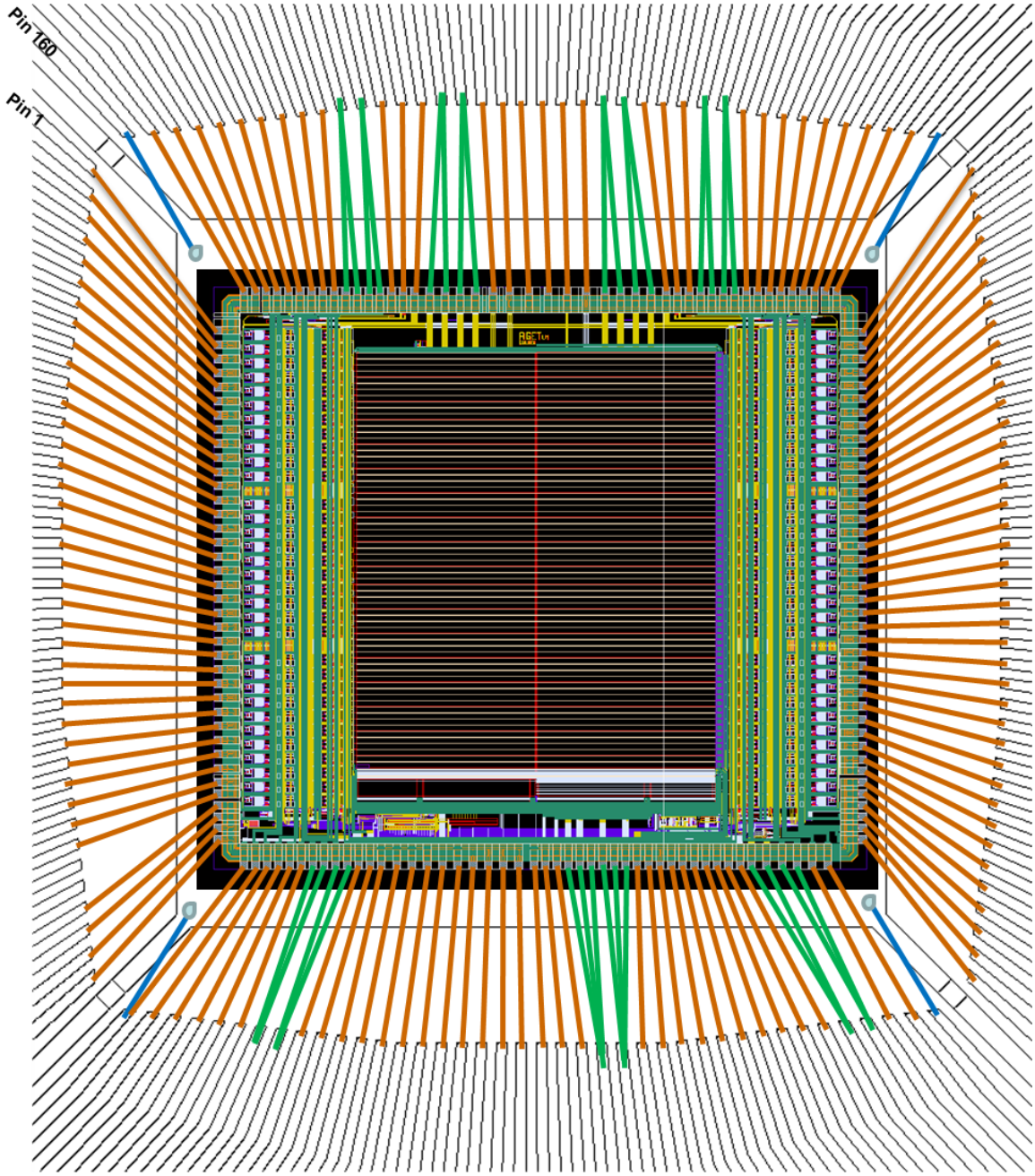


Fig. 90: Bonding diagram of the AGET chip.

A double bonding is necessary for the package pin numbers: 41, 47, 48, 76, 77, 131, 132, 136, 137, 144, 145, 149 & 150.

A triple bonding for the package pin numbers: 64 & 65.

The package pin numbers: 41, 80, 121 & 160 are used to supply the cavity of the package (ASIC substrate).

The package pin numbers: 35 & 36 are not connected.

Annexe 4: AGET input impedance & external coupling mode

This document gives some rules about the use of AGET ASIC in particular cases where the chip is coupled to a detector or protection devices, or to external electronic as external CSA with highest dynamic.

Contents

1.0 Characterization of AGET input channel

The particularity of the channel input is to be polarized to a voltage defined by the gate to source voltage of CSA input transistor. This transistor is a NMOS, with source connected to VSS, and its gate voltage depends to its current value defined externally by specific pads (122/155) and internally by slow control (factor 2 or not by state1<0>). The **Fig. 91** gives the value of this voltage versus NMOS current. This feature does not allow DC coupling with external supplied system.

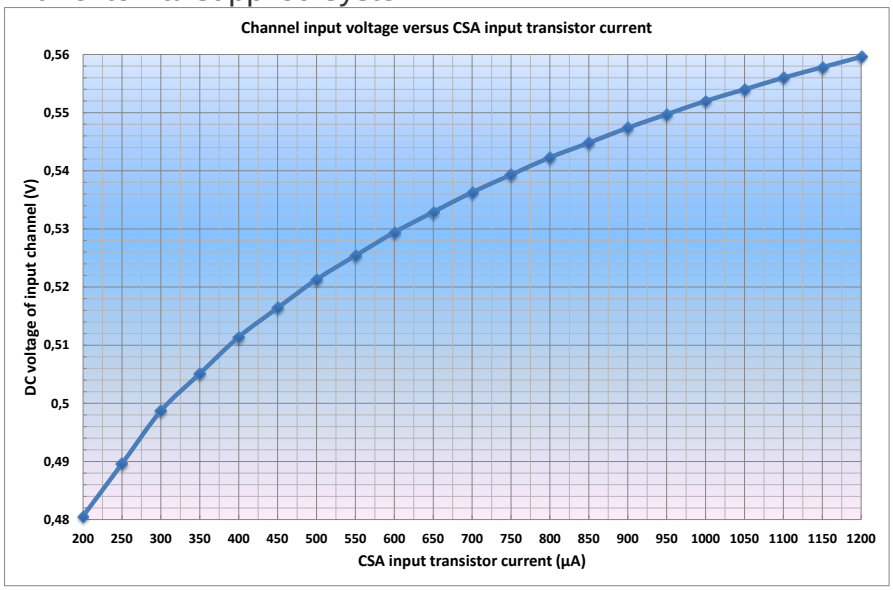


Fig. 91: Channel input voltage versus CSA input current.

For the DC current, the ASIC can provide or absorb up to a specific range. This range is dependent on the CSA gain, since there is one resistor value per gain in order to have a constant integration time of 50 µs. The **Fig. 92 to 95** show the different ranges according to the value of gain and polarity of detector signal.

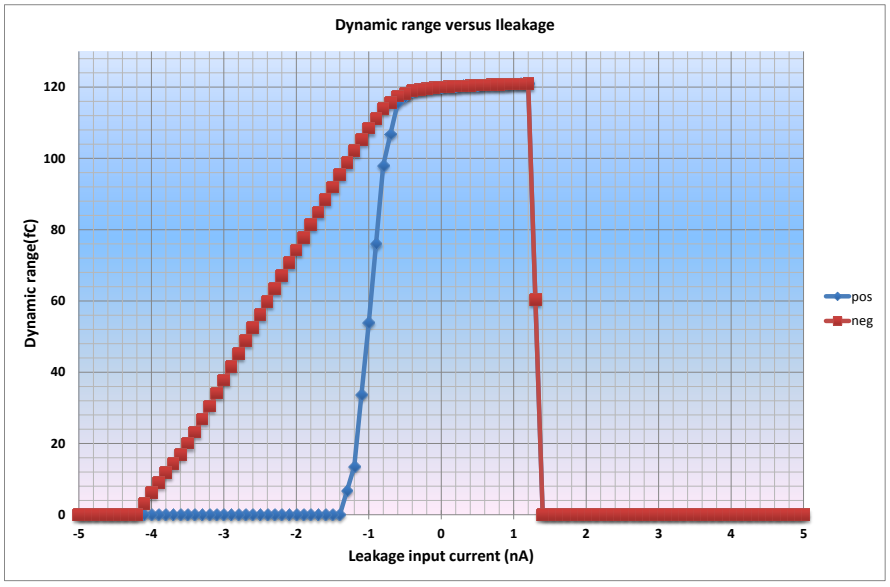


Fig. 92: Dynamic range versus leakage current and polarity for 120 fC range.

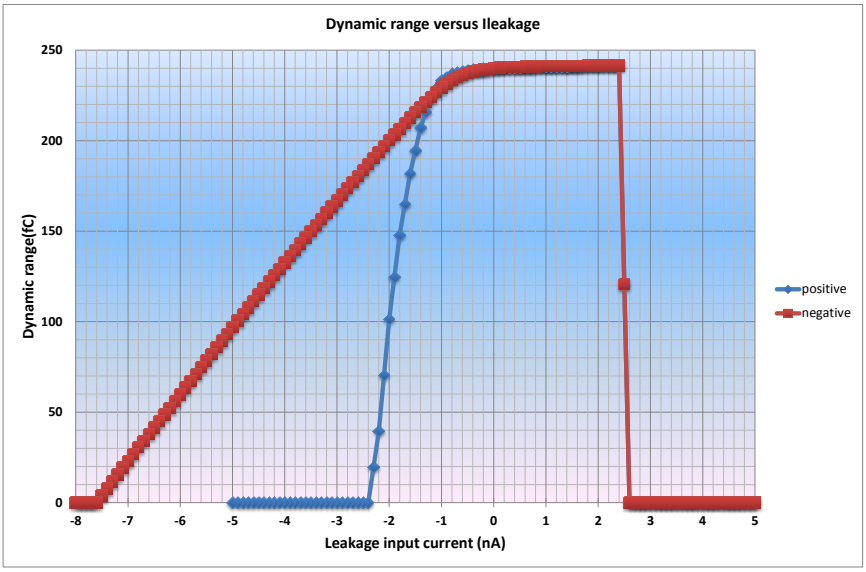


Fig. 93: Dynamic range versus leakage current and polarity for 240 fC range.

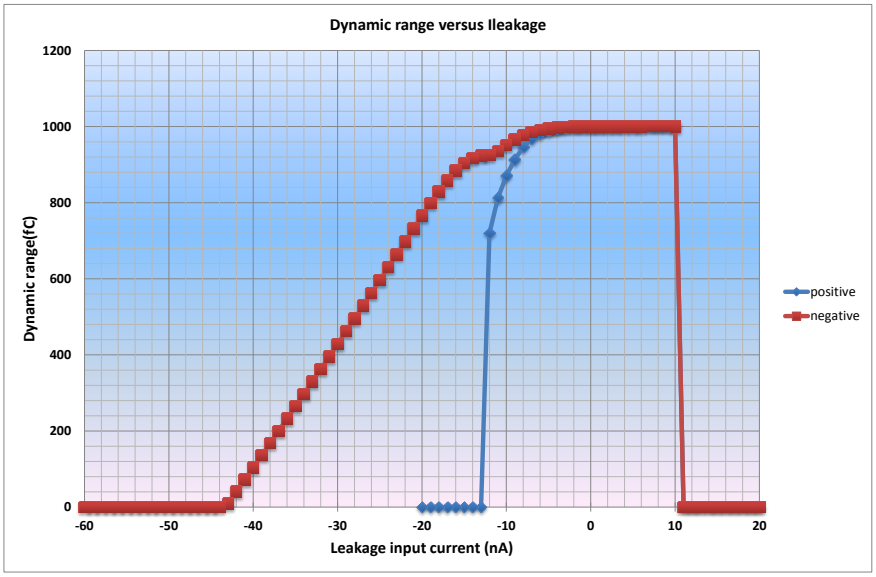


Fig. 94: Dynamic range versus leakage current and polarity for 1 pC range.

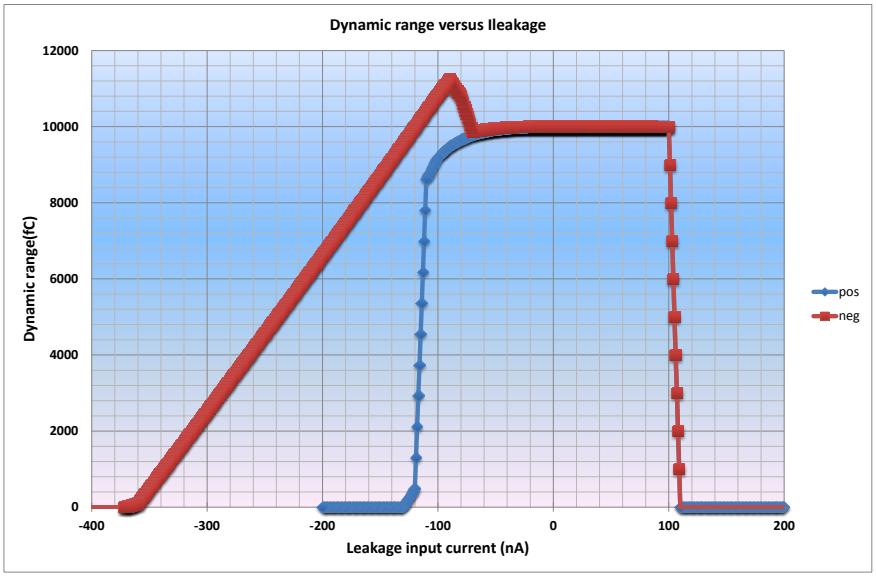


Fig. 95: Dynamic range versus leakage current and polarity for 10 pC range.

If the current is too high, the CSA will be in a saturated state and therefore will be nonfunctional. This default can arrive if the ASIC is DC coupled to a detector with high leakage current (Silicon detector) or TPC with sparks protection system.

Concerning these protections, a system with 2 diodes is generally used (**Fig. 96**), placed directly to the ASIC input.

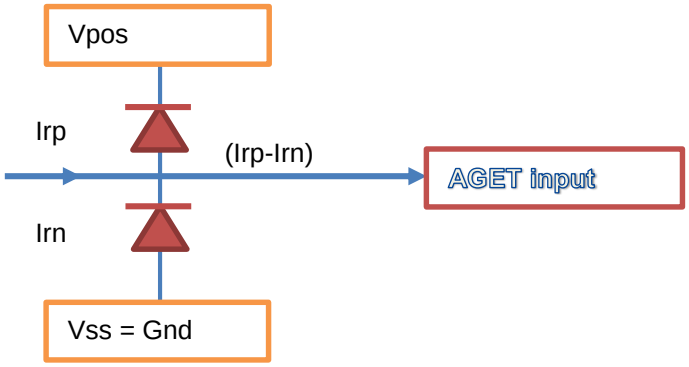


Fig. 96: Schematic of input protection.

This configuration implies therefore a sensitivity of the CSA to the difference of reverse current going through the two protection diodes. This reverse current is strongly dependent on the temperature, bias voltage and manufacturer. For AFTER ASIC, which has the same input stage as the one of AGET, the BAV99W diodes pairs from INFINEON has been choose with bias voltage of the “up” diode fixed to 1.1 V, given a satisfactory margin in temperature for use at 50 ° C maximum.

2.0 Input impedance of AGET

The input impedance depends of two parameters:

- Charge range (4 possible charge ranges: 120 fC, 240 fC, 1 pC & 10 pC)
- Current value of CSA input transistor (400 µA & 800 µA)

The input impedance is described in the **Fig. 97**.

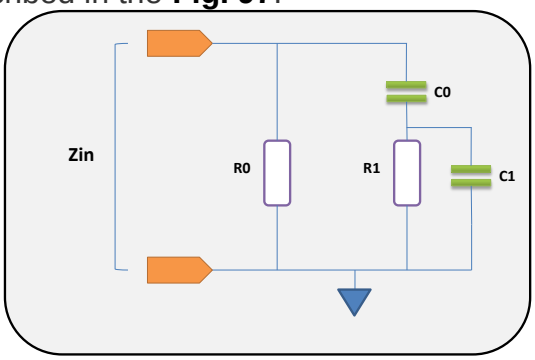


Fig. 97: Input impedance schematic of AGET.

The value of each component is reported in the table 45.

	120 fC		*240 fC*		*1 pC*		*10 pC*	
ICSA	***R0***	***R1***	***R0***	***R1***	***R0***	***R1***	***R0***	***R1***
400 µA	111k	700	62k	500	12.7k	200	7.28k	140
800 µA	107k	400	60k	300	12.27k	120	5.53k	80
C0	310p		580p		3n		8n	
C1	4p		2p		3p		2p	

Table 45: Values of input components.

3.0 Characterization of AGET input channel in external mode (external CSA)

In AGET ASIC, the user has the possibility to connect external electronic (**Fig. 98**) through input channel directly to the input of SK filter or GAIN -2.

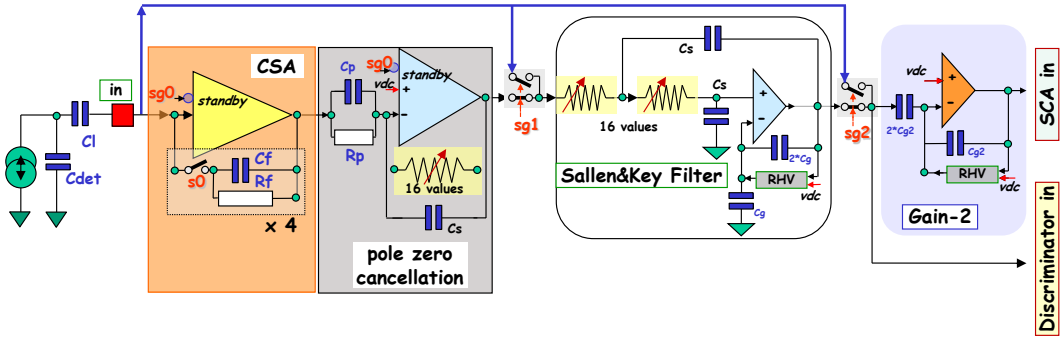


Fig. 98: Schematic of AGET front-end channel.

This implies to bypass the internal CSA or the SK filter by programing the 2-bit registers state1<31:30> as described in table 46.

State1<31>	State1<30>	Access point
0	0	none
0	1	SK filter input (CSA standby mode)
1	0	GAIN -2 input (CSA standby mode)
1	1	CSA standby mode

Table 46: Selection of access point in external mode.

Therefore, the user must take into account the input dynamic range, the input polarity and DC input voltage of the SK filter and GAIN -2.

3.1 SK filter

The filter (**Fig. 99**) is 2-complex pole Sallen-Key low pass filter. The available range of peaking time extends from 50 ns to 1 µs (sixteen values) defined by state1<6:3>.

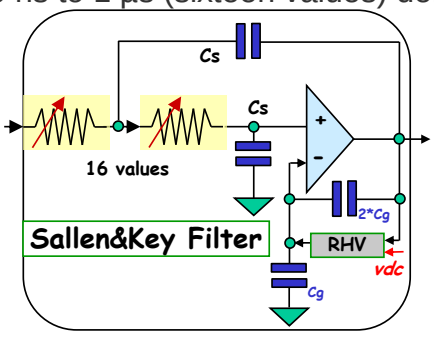


Fig. 99: Schematic of SK filter.

The DC output voltage value is defined internally and controlled by the polarity bit state1<16> (“0”: 2.2 V; “1”: 0.7V). The input DC level must be set to a level compatible with the polarity defined in AGET by the state1<16> (table 47) and the input dynamic range.

State1<16>	SK input signal polarity	DC input level	Input dynamic range
0	negative	2.2 V – 0.7 V	- 480 mV max.
1	positive	0.7 V – 2.2 V	+ 480 mV max.

Table 47: Input polarity and voltage dc level for SK filter.

3.2 Gain -2

This gain provides an extra x2 inverting voltage gain and the necessary buffering for the signal sampled in the SCA (**Fig. 100**).

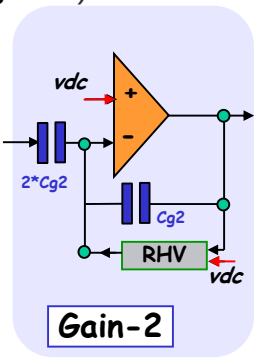


Fig. 100: Schematic of GAIN-2.

Its total output dynamic (full range) is 1.5 V. The DC output voltage is defined internally by the polarity bit state1<16> (“0”: 0.7 V; “1”: 2.2V). The DC input voltage must be set to a level compatible with the polarity defined in AGET by the state1<16> (table 48) and the input dynamic range.

State1<16>	GAIN-2 input signal polarity	DC input level	Input dynamic range
0	negative	2.2 V – 0.7 V	- 750 mV max.
1	positive	0.7 V – 2.2 V	+ 750 mV max.

Table 48: Input polarity and voltage dc level for GAIN-2.

4.0 Both polarity of the input signal in external mode (input GAIN -2 configuration)

As describe previously, the chip can be used only for its SCA by bypassing the CSA & filter and entering directly to the input of GAIN -2 stage. In some case, the input signal can be bipolar (positive and negative) and is not compatible with the nominal setup of the chip since the DC voltage of stages is defined internally and adjustable for positive or negative polarity of the signal. But it is possible to adjust this value by putting external resistor on the AsAd card or PCB support card of AGET since the internal DC voltages are accessible through dedicated pads of the chip.

According to the internal choice of the signal polarity through the state1<16>, a resistor must be placed between each pads Vdc_g2d (Pin n° 135) & Vdc_g2g (Pin n° 146) and Vdd (3.3 V) or gnd (0 V) as presented in the **Fig. 101** and table 49.

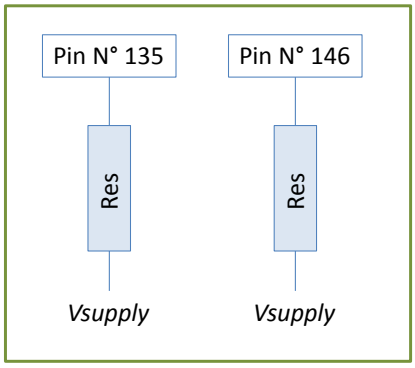


Fig. 101: Schematic of external DC supply of GAIN-2.

With these values we obtain a DC voltage value of the GAIN -2 output of 1.45 V (2.2 V or 0.7 V without external resistor) compatible with the both polarity of the signal.

State1<16>	detector polarity	Resistor value	Vsupply
0	negative	5.13 K	3.3 V
1	positive	6.842 K	0 V

Table 49: Value of external resistor.

Annexe 5: AGET chip in positive polarity mode

Since the beginning of the GET project, all the studies, analysis and measurements have been mainly done in the negative polarity mode. The raison is that the majority of the TPC used by the GET collaboration are readout by micro pattern readout using Micromegas or GEM technology. Of course, the functionality has been checked for the positive polarity mode but unfortunately not for all the possible modes of chip functionality (four gains; sixteen peaking time values and CSA current).

At the end of 2014, some anomaly in the gain uniformity of AGET was identified for the first time by TadaAki Isobe from RIKEN if the GET electronic is configured in positive polarity mode. Additional measurements have been performed at IRFU to understand the problem and a note has been written (AGET_POSITIVE_POLARITY_NOTE.pdf; ref: GET-QA-000-0011; December 03, 2014) explaining that the charge delivered in the functionality test mode was not uniform for all channels and should be avoid if users plan to use it for measurement purpose. This analysis has been made for the gain configuration in calibration mode (1pC) for which good gain uniformity was achieved. The new data from TadaAki Isobe have pushed us to made exhaustive test on the chip showing effectively the non-uniformity of the chip for the three other gains.

The purpose of this document is to present the problematic of the AGET chip in the positive polarity mode in the actual setup and to propose a simple solution to resolve it.

Contents

1 Problem description

In the actual set-up of GET electronic, a non-uniformity of the gain between channels can be observed if the polarity of the input signal is positive. A good illustration of the problem is reporting in the **Fig. 102** corresponding to the response of 64 channels (+ 4 FPN channels) to the “same” electrical charge in the functional test mode.

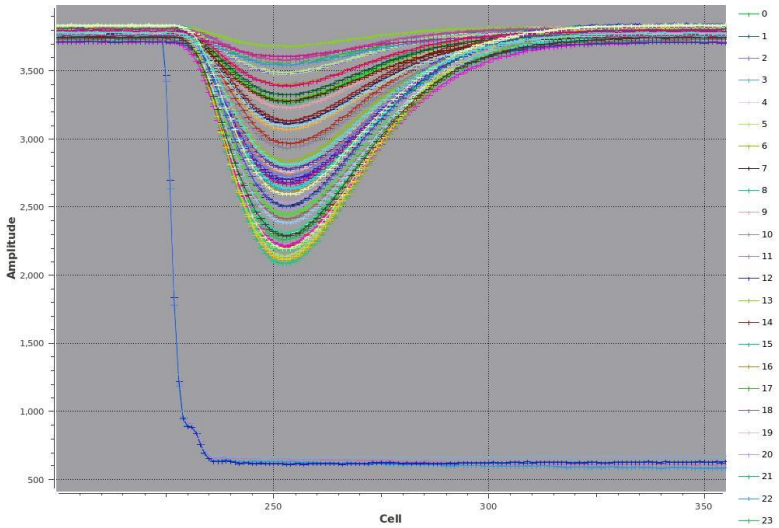


Fig. 102: SCA signals in functional test mode for the 120 fC range.

This abnormal behavior is also obtained independently of the internal test mode choice (functional, test or calibration) or external test system using external pulsing test board (external injection capacitor and generator).

In the **Fig. 103** are reported the slope of the transfer function of the 64 channels in functional test mode for 2 gains (120 fC & 240 fC) and for the both polarities. ***The problem concerns few channels and depends on the gain value***.

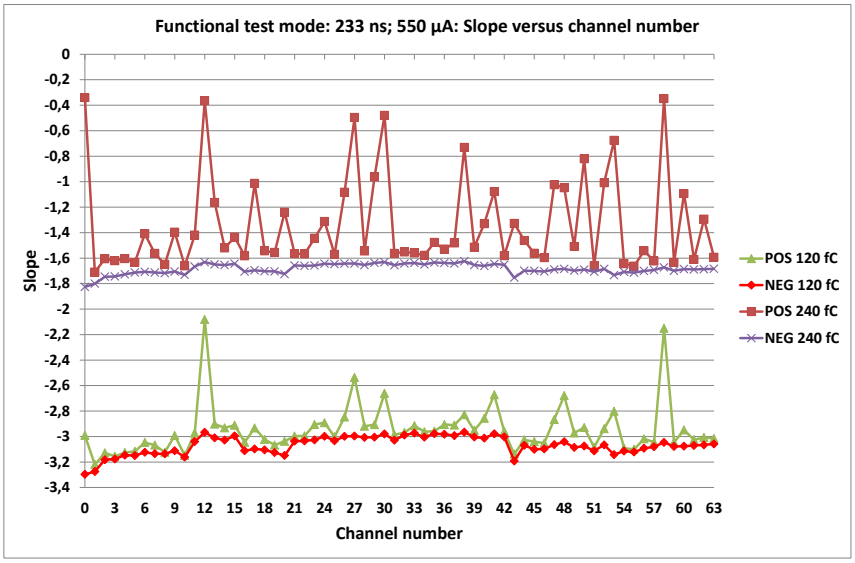


Figure 103: Gain obtained for the both polarities in functional test mode for 120 & 240 fC charge ranges.

In the **Fig. 104** are reported for the same ASIC, the slope of the transfer function of the 64 channels in calibration test mode for 2 gains (120 fC & 240 fC). The non-uniformity of the gain is obtained on the same channels.

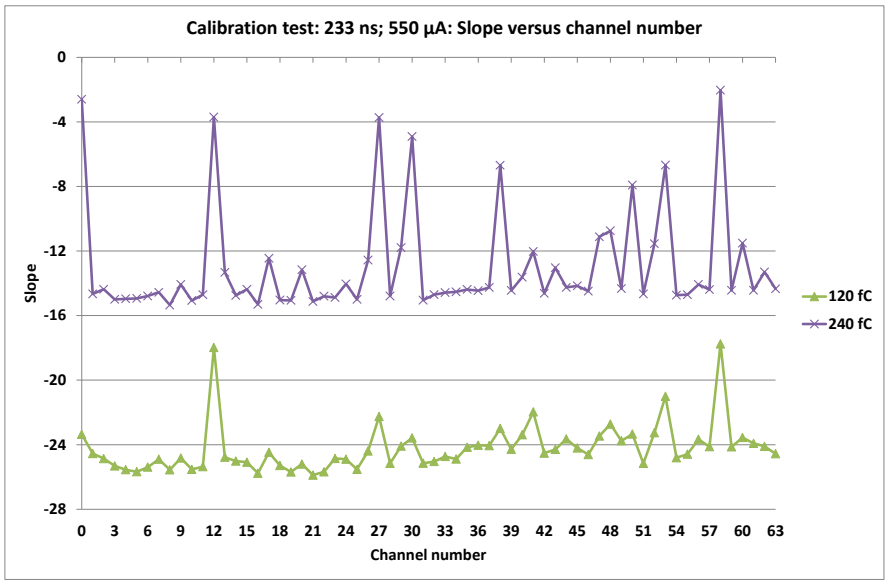


Figure 104: Gain obtained in calibration mode for the 120 fC & 240 fC ranges.

In **Fig. 105** are plotted the maximum amplitude of the 64 SCA signals corresponding to an injection charge through external generator & calibration capacitors. These results are obtained from the same ASIC and for the 120 fC range. The lowest amplitudes correspond to the channels which present the lowest transfer function in the previous tests (figure 2 to 3).

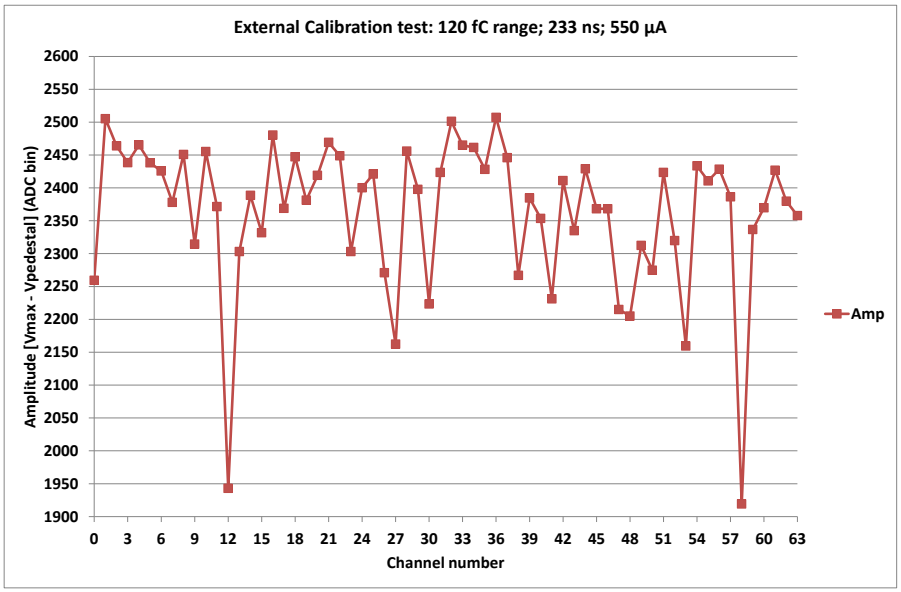


Figure 105: Amplitude obtained in external calibration mode for the 120 fC range.

This non-uniformity exists for all the AGET chips at different levels, independently of channel number. The **Fig. 106** shows the results obtained for 2 different ASICs.

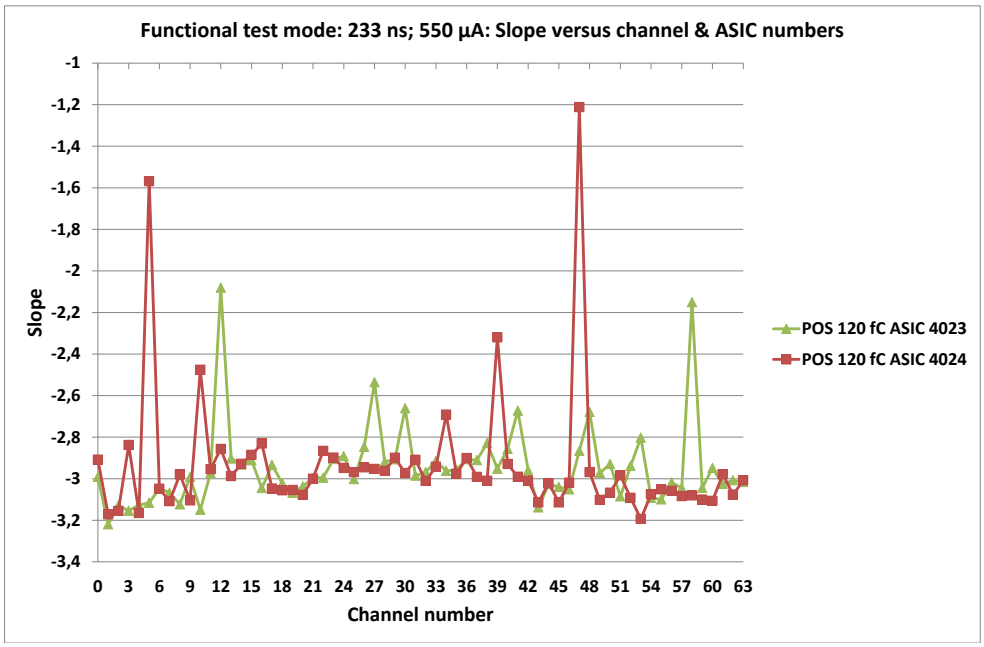


Figure 106: Gain obtained in functional test mode for 2 ASICs.

The level of the non-uniformity depends on the selected range and could be in some case non-existent. In the **Fig. 107** are reported the gain obtained in calibration mode for the 1 pC range showing a good uniformity.

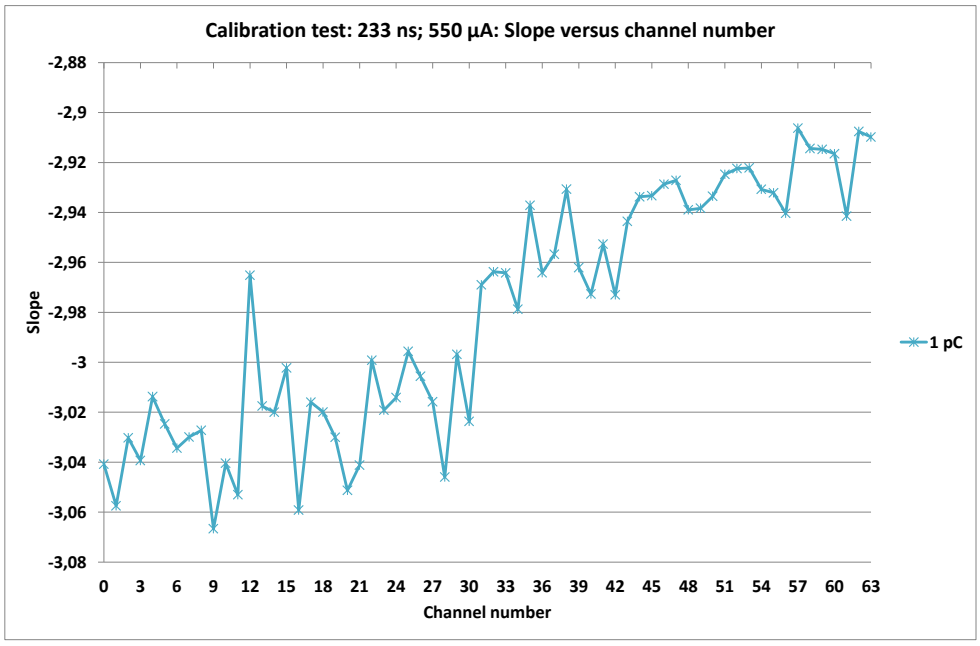


Figure 107: Gain obtained in calibration mode for the 1 pC range.

2 Origin of this anomaly

A campaign of tests has been done at IRFU showing that ***the non-uniformity in positive mode came from bad value of the CSA output DC voltage***. The CSA output DC voltages have been measured for different ASICs and charge ranges and are reported in the table 50. These values concern only the channel 0, measured through the DEBUG pad.

	120 fC	240 fC	1 pC	10 pC
ASIC 3999	2.91 V	2.94 V	2.65 V	2.76 V
ASIC 4023	2.936 V	2.95 V	2.79 V	2.95 V
ASIC 4024	2.97 V	2.95 V	2.79 V	2.96 V

Table 50: CSA output DC voltage value versus charge range & ASIC in positive polarity mode.

These values are for the faulty channels ***highest than the 2.8 V attempt*** putting their CSA in degraded functional mode These values confirm the loss of gain for the 3 charge range 120 fC, 240 fC & 10 pC and normal value for the 1 pC range. We can notice also a ***high spread of the CSA output DC voltage*** (400 mV max.).

To confirm the diagnostic of the failure, ***Monte-Carlo simulations*** have been done on the design to take into account the effect of technology parameter variations or non-matching process on the values of CSA output DC voltage. For technology parameter variations, the highest fluctuations (table 51) are obtained for the 1 pC & 10 pC ranges but remain acceptable.

	120 fC	240 fC	1 pC	10 pC
Mean value	2.836 V	2.870 V	2.827 V	2.803 V
Sigma	6.13 mV	6.23 mV	28.57 mV	26 mV

Table 51: Monte-Carlo simulation. Effect of technology parameter variations on CSA DC voltage value in positive polarity mode.

*For Monte-Carlo simulations taking into account the matching parameter****, the effect is much important and results (table 52) are similar with the measured data.***

	120 fC	240 fC	1 pC	10 pC
Mean value	2.83 V	2.87 V	2.84 V	2.80 V
Sigma	45 mV	52 mV	51 mV	74 mV

Table 52: Monte-Carlo simulation. Effect of matching parameter on CSA DC voltage value in positive polarity mode.

Another point concerns the relative dispersion between the 4 gains which is in part confirmed by the simulation. The **Fig. 108** shows the variation of the DC value for the 4 gains which can go from 40 mV to 240 mV. These values are less that the 400 mV obtained on some channels of some ASICs which prove the difficulties at the design level to detect and to take into account these phenomena.

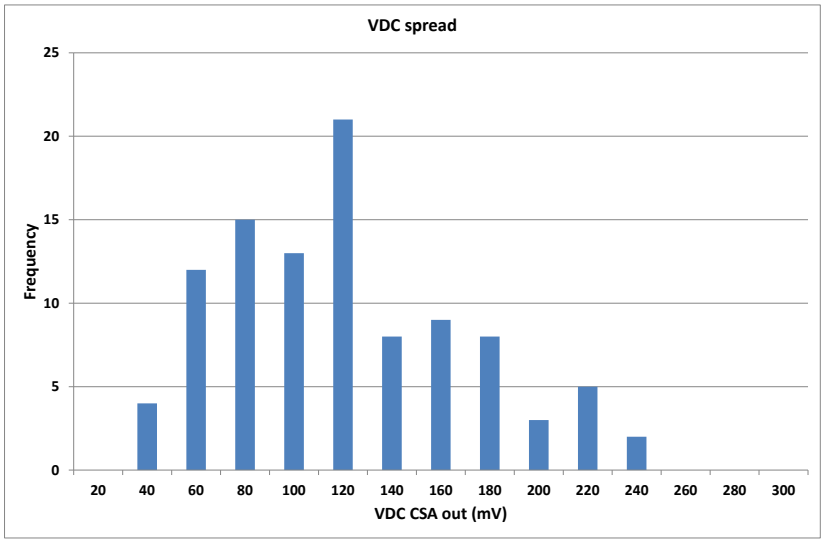


Figure 108: Monte-Carlo simulation. Effect of the matching parameter on the dispersion of CSA DC voltage values between the 4 gains.

These DC fluctuations or offset have some consequence on the polarization of the CSA and therefore on its functionality. Simulations have been made in transient time analysis to evaluate the sensitivity of the front-end to the value of CSA DC output voltage. The **Fig. 109** shows the amplitude of the ADC differential input signal according to the values of CSA DC voltage and input charge.

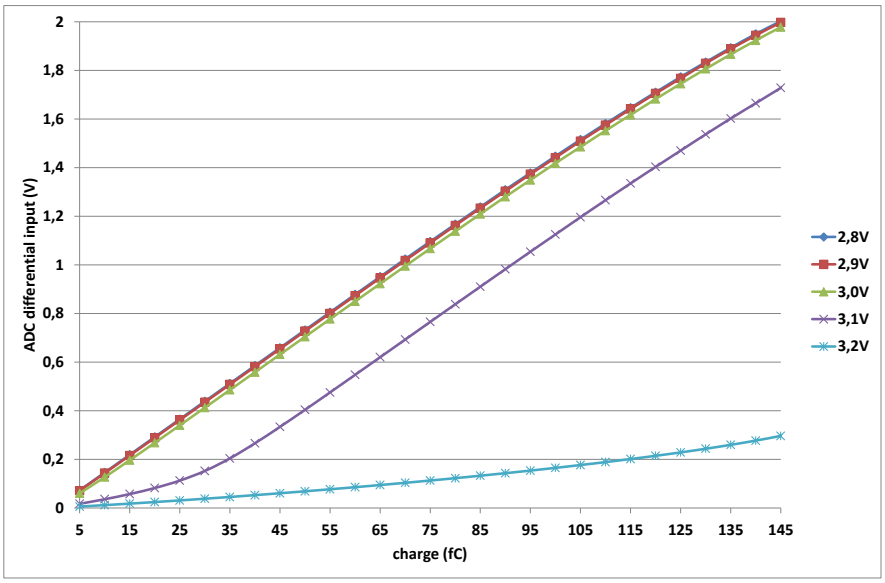


Figure 109: Amplitude of ADC differential signal input versus CSA DC voltage & input charge for the 120 fC range in positive polarity mode.

3 Solution

This DC value is by default defined inside the chip. According to the input polarity, this DC value is automatically changed inside the chip (by slow control) and adjusted to 1.8 V in negative mode or 2.8 V in positive mode. The same process is also done for the other functional blocks of the channel (0.7 V to 2.2 V or 2.2 V to 0.7 V).

But ***this value (as the others) can be modified externally since this voltage is accessible through specific AGET pads***. For the CSA output DC voltage, there are 2 pads: pad 133 (Vdc_csad) & pad 148 (Vdc_csag). This value can be controlled by putting external resistor on each 2 pads referenced to the ground. The resistor values must be equal to ***10 kΩ*** to have a DC value of 2.4 V (**Fig. 110**).

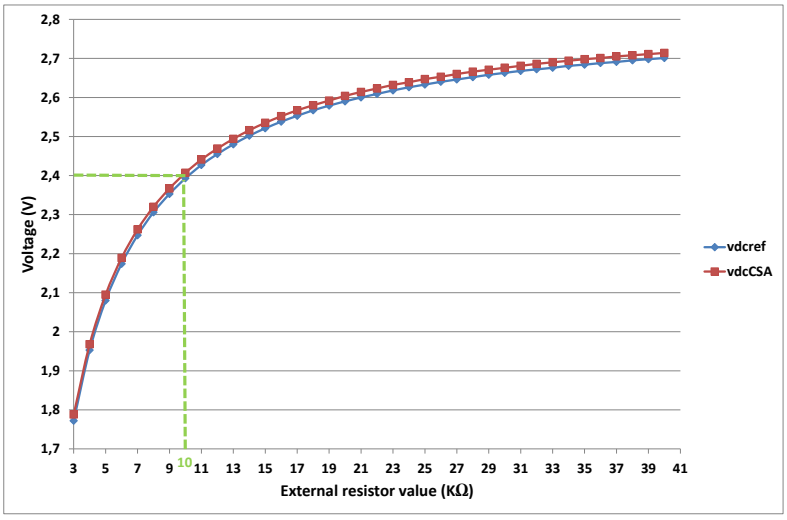


Figure 110: Reference DC value versus external resistor value (Simulation).

This value given by simulation was also confirmed by measurement on a high number of ASICs (50). For the 120 fC range, the functional test mode is used to extract the slope of transfer function. These results are plotted in the **Fig. 111** and can be compared with the ones in the **Fig. 112** extracted previously at “nominal” 2.8 V with the test bench.

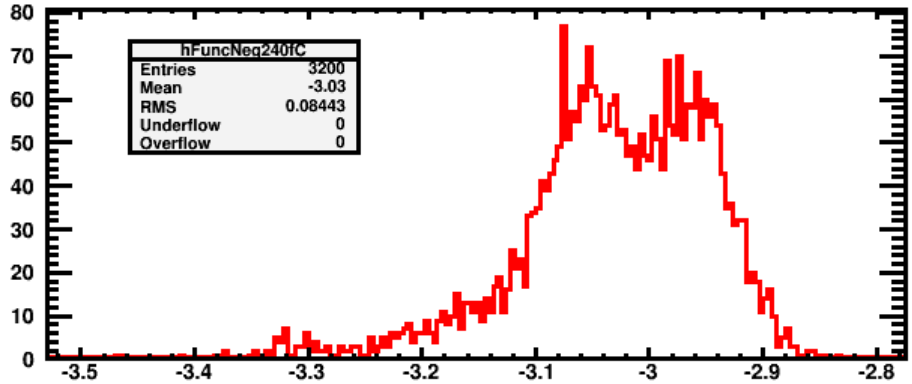


Figure 1: Slope obtained on 50 ASICs in functional test mode for the 120 fC range and at 2.4 V.

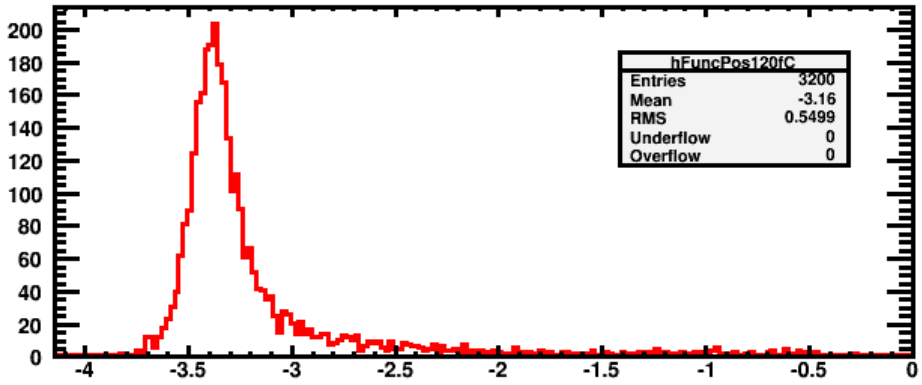


Figure 112: Slope obtained on 50 ASICs in functional test mode for the 120 fC range and at 2.8 V.

The gain of the chips at 2.4 V is much more uniform and conforms to the one obtained in negative polarity mode (**Fig. 113**). The main value is different since the peaking time measured at 2.8 V case was programmed at 1 µs.

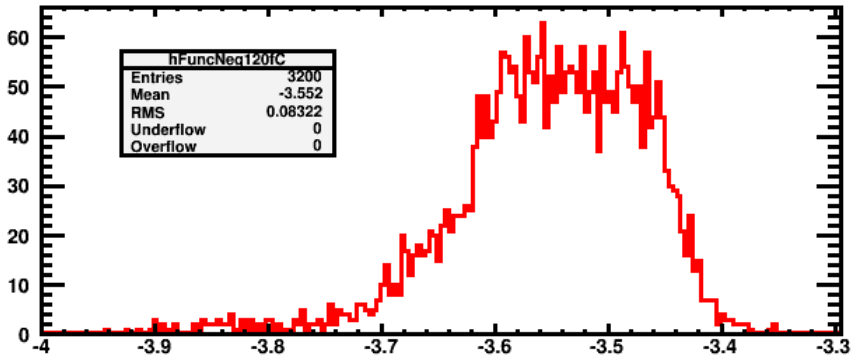


Figure 113: Slope obtained on 50 ASICs in functional test mode for the 120 fC range at 2.8 V and in negative polarity mode.

To modify the CSA DC value, it is necessary to ***modify the actual AsAd V2.1 card by putting these 8 resistors at the place of the 8 decoupling capacitors*** (**Fig. 114**).

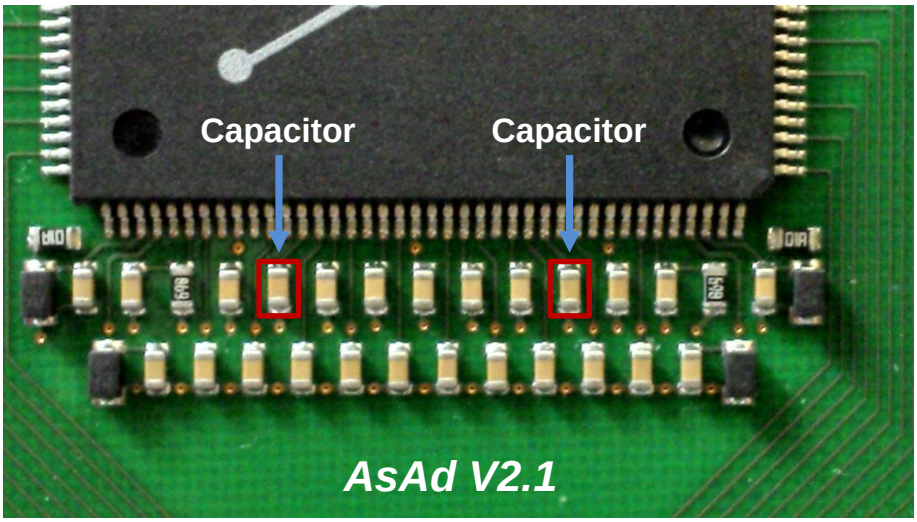


Figure 114: Location of the 2 decoupling capacitors on V2.1 AsAd card.

Measurements have been made to evaluate the noise without decoupling these 2 points. These results are reported in the **Fig. 115** obtained for the most critical gain (120 fC) and for different peaking time values.

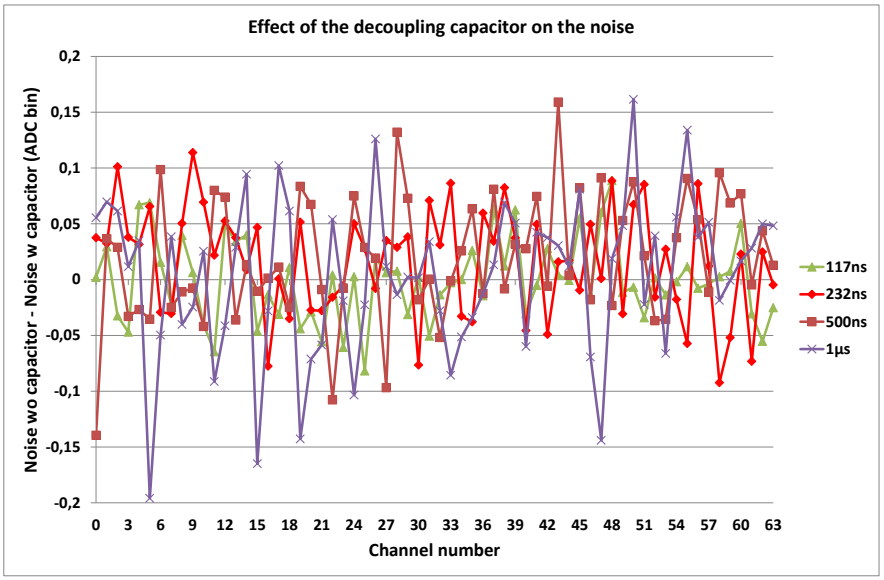


Figure 115: Noise difference between a configuration without and with decoupling capacitor. Charge range is 120 fC.

These results show that these decoupling capacitors have any impact on the noise and can be therefore replaced by the resistors.

These resistors are also any impact on the AGET functionality in the negative polarity mode. Effectively instead to have 1.8 V, we will have something around 1.51 V (**Fig. 116**). The blue curve corresponds to modified internal reference voltage and the red curve to the CSA output DC value. We can notice that the CSA DC voltage cannot go down to a voltage less than 1.5 V.

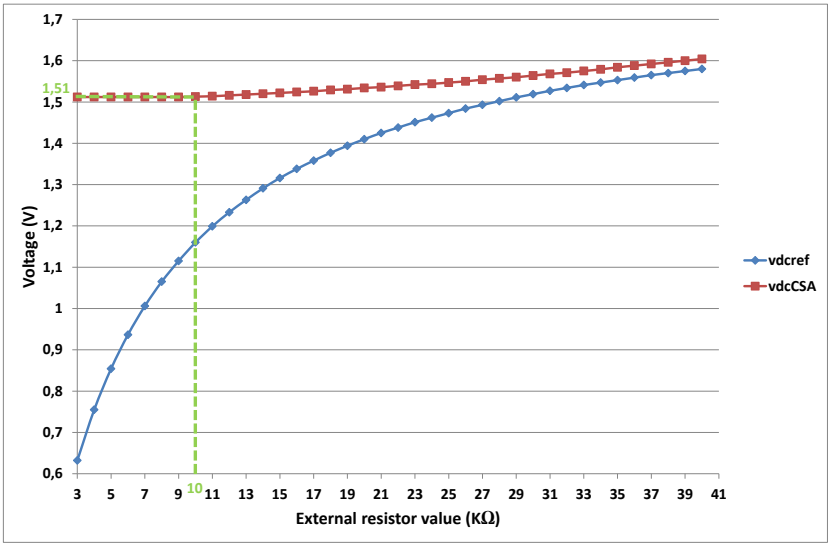


Figure 116: REF & CSA DC voltage values versus external resistor in the negative polarity mode.

Measurements have been made for the previous and new setup and the main results (table 53) obtained on 50 AGETs are similar and show the full functionality of the chip.

	1.8 V			1.5 V		
	min	**max**	**var (%)**	**min**	**max**	**var (%)**
Noise	2.85	4.26	***+/- 19.8***	2.7	4.36	***+/- 23.5***
FPN Noise	1.61	1.89	***+/- 8***	1.6	1.92	***+/- 9***
Calibration	-4.37	-3.88	***+/- 5.9***	-4.38	-3.99	***+/- 4.7***
Threshold						
min	4	12	***+/- 50***	3	10	***+/- 53***
5%	45	56	***+/- 11***	47	62	***+/-13***
18%	14	20	***+/- 17***	14	22	***+/- 22***
5% pos	1	47	***+/- 96***	37	52	***+/- 17***

Table 53: Test results obtained for 2 values of CSA DC voltage: 1.8V & 1.5 V. 50 ASICs & negative polarity mode.

4 Conclusion

It has been shown that the AGET chip cannot operate reliably in the positive polarity without adding external components. Analysis has shown that it is because of the CSA internal DC voltage which is not well defined for some channels. To correct it, an external resistor must be soldered on AsAd board at the place of decoupling capacitor. The test performed and simulation indicate that this modification can be done on the future AsAd board which will permit to have a unique system compatible with the both input signal polarities.

Annexe 6: Note on the Multiplicity signal

This note gives some recommendations about the tuning of multiplicity signal amplitude through the slow control register.

The unity amplitude and the width of the multiplicity signal can be adjusted by setting the 2-bit AGET slow control register state1<28:29>, called ***Bit lsb_trigg_width to msb_trigg_width*** or ***Triggwidth0 to 3*** at system level. This feature permits to control the 2 parameters width & amplitude according to the process corners. The configuration "00" corresponds to a reference value which can be decreased or increased with the 3 other configurations as shown in table 54.

Triggwidth	Width range: 100 ns	Width range: 200 ns	Amplitude
Triggwidth0	Value100nswidth0	Value200nswidth0	ValueAmpwidth0
Triggwidth1	-17 %/Value100nswidth0	-22 %/Value200nswidth0	-25 %/ValueAmpwidth0
Triggwidth2	+18 %/Value100nswidth0	+8 %/Value200nswidth0	+25 %/ValueAmpwidth0
Triggwidth3	+36 %/Value100nswidth0	+36 %/Value200nswidth0	+50 %/ValueAmpwidth0

Table 54: Adjustment of Multiplicity width & amplitude.

But the choice of the configuration can have an impact on the multiplicity amplitude measurement especially if the unity value is too high. If it is the case, the pedestal of the multiplicity signal can be outside of input dynamic range of the ADC (1 V to 2 V) prohibiting the conversion of multiplicity level less than 2 (3 if unlucky).

For the AGET production test bench, the parameter for ***Triggwidth*** is fixed to ***Triggwidth2*** to cope with the ADC input dynamic range with enough margins. In **Fig. 117** is reported the pedestal value measured on 908 AGET ASICs. The mean value is 189.4 ADC bin (29.68 ADC bin of sigma).

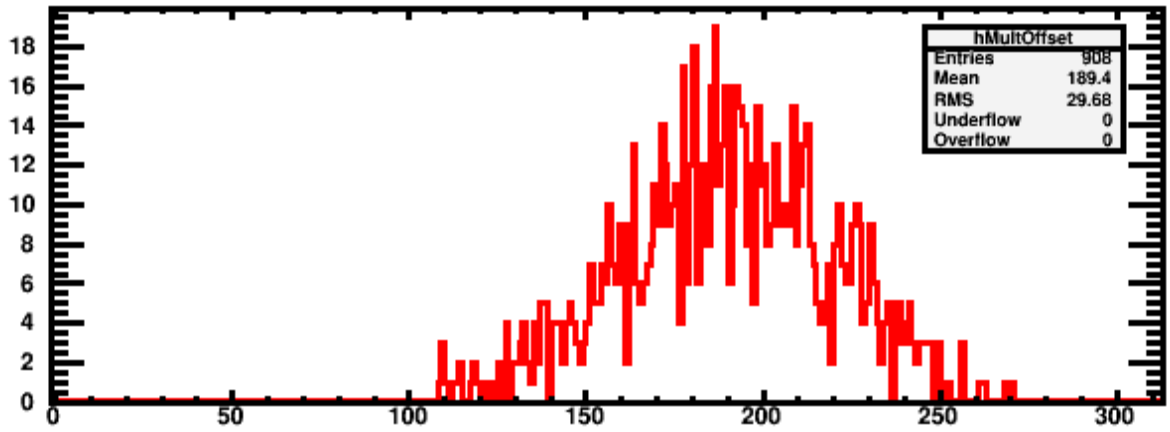


Figure 117: Multiplicity offset measured on 908 AGETs.

The slope of transfer function (**Fig. 118)** is 56.44 ADC bin per hit channel (0.736 ADC bin of sigma).

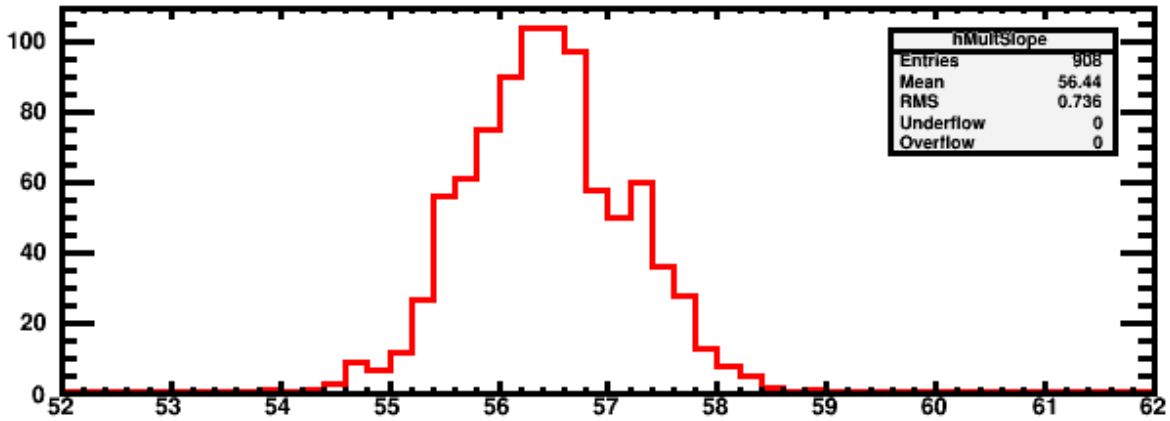


Figure 118: Slope of multiplicity transfer function obtained on 908 AGETs.

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