Technical Information Manual

Revision n. 1
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MOD. C 205

32-CHANNEL CHARGE-INTEGRATING ADC (CIA)

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. Description

1.1. Functional description

The CAEN Model C 205 32-CHANNEL CHARGE INTEGRATING ADC (CIA) is a single width CAMAC module provided with 32 independent input channels.

The functional block diagram of the module is shown in Fig. 1.1, p.5.

For each channel, the input charge, received when the GATE signal is active, is converted to a voltage level through a Charge to Voltage Converter (CVC); each CVC output voltage is then amplified by both a 1X-gain amplifier and a 7.5X-gain amplifier, and sequentially transformed into two corresponding 12-bit words through two parallel 12-bit Analog to Digital Converters (ADC): the word generated by the ADC following the 7.5X-gain amplifier corresponds to 15 bit resolution.
At the same time a BUSY output signal is available at the corresponding pins of the 10-pin front panel connector.

Each couple of words corresponding to a conversion value is stored into a RAM-type internal memory (readable via CAMAC) in sequential order.

At the end of the analog-to-digital conversion of the last input signal, a LAM signal is generated. At this point the conversion values corresponding to each input charge can be read via CAMAC.

The "TEST" input connector allows the user to perform test operation by using a single input signal common for all channels.

The **Model C 205** is available in three different versions which differ from each other for the input signal characteristics:

- **Mod. C 205 N** – has 32 channels with 50 Ω input impedance and accepts single-ended negative input signals.
- **Mod. C 205 P** – has 32 channels with 50 Ω input impedance and accepts single-ended positive input signals.
- **Mod. C 205 D** – has 32 channels with 110 Ω input impedance and accepts differential input signals.

The **Model C 205 A** (also available in three different versions, see below) is exactly the same as the Mod. C 205 except that it is a double CAMAC unit wide module with only 16 channels and 00-type LEMO connectors on the front panel instead of the 32+32 pin flat cable-type connector.

- **Mod. C 205 AN** – has 16 channels with 50 Ω input impedance and accepts single-ended negative input signals.
- **Mod. C 205 AP** – has 16 channels with 50 Ω input impedance and accepts single-ended positive input signals.
- **Mod. C 205 AD** – has 16 channels with 110 Ω input impedance and accepts differential input signals.

All the versions available for the Mod. C 205 and Mod. C 205 A are summarised in Table 1.1.

Table 1.1 – Versions available for the Mod. C 205 and Mod. C 205 A

Model	Input channels	Input signal polarity	Impedance
C 205 N	32	Single-ended negative	50 Ω ± 1.5%
C 205 P	32	Single-ended positive	50 Ω ± 1.5%
C 205 D	32	Differential	110 Ω ± 1.5%
C 205 AN	16	Single-ended negative	50 Ω ± 1.5%
C 205 AP	16	Single-ended positive	50 Ω ± 1.5%
C 205 AD	16	Differential	110 Ω ± 1.5%

(This module is a CERN design).

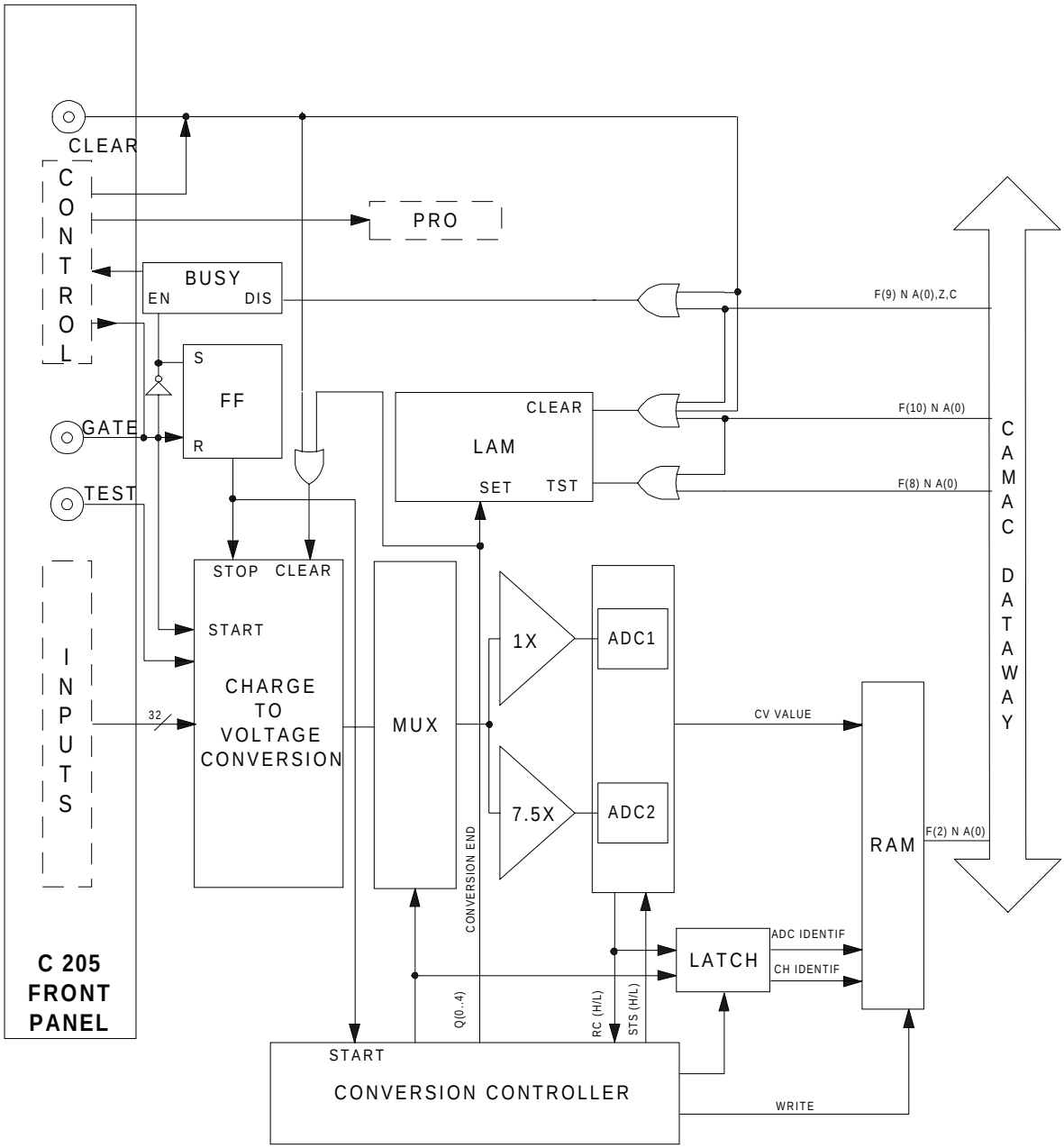

Fig. 1.1 – Functional block diagram of the module

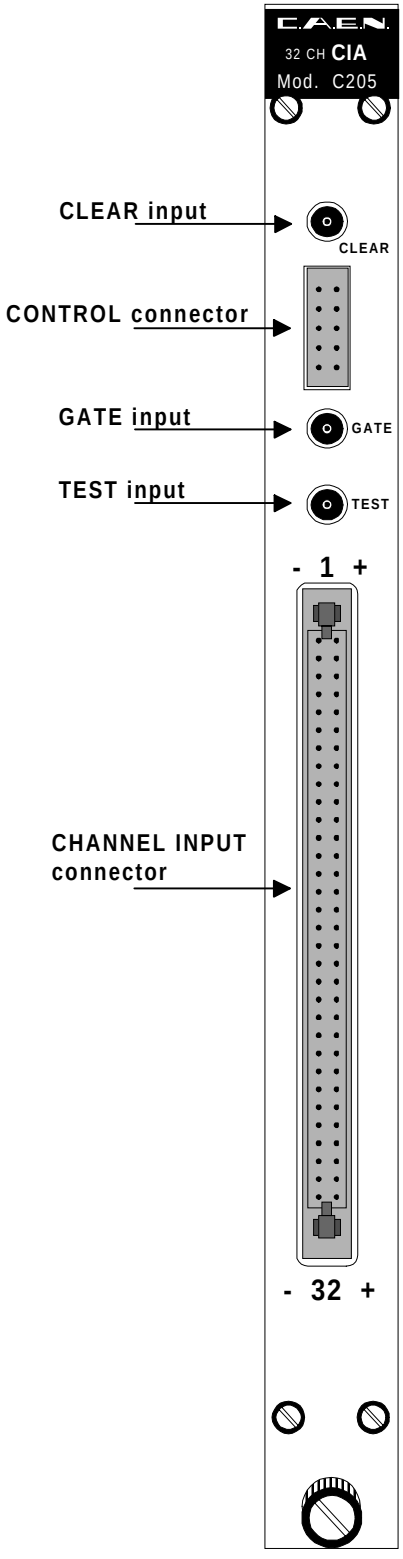

Fig. 1.2 – Mod. C 205 front panel

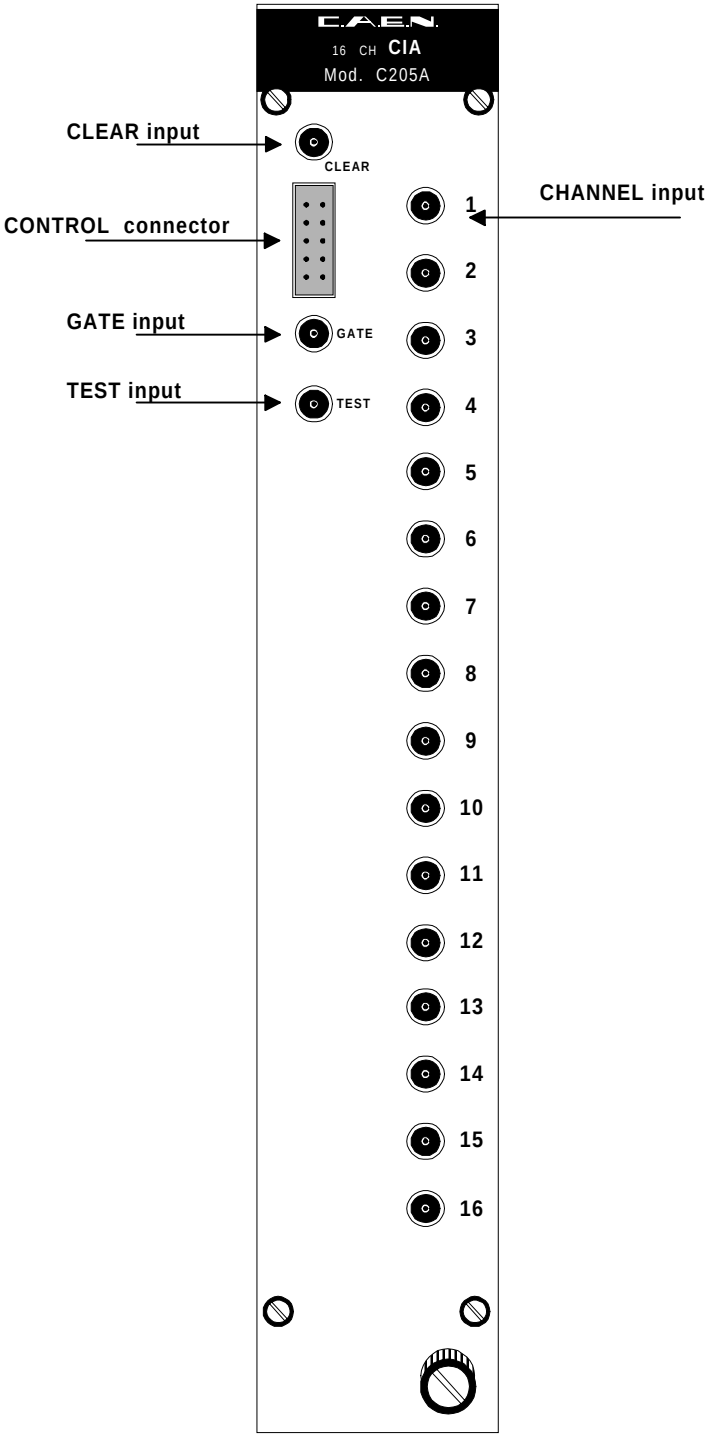

Fig. 1.3 – Mod. C 205 A front panel

2. Technical specifications

2.1. Packaging

The Mod.C 205 is housed in 1-unit wide CAMAC module.

The Mod. C 205 A is housed in a 2-unit wide CAMAC module.

2.2. Power requirements

+6 V	490 mA
–6 V	430 mA
+24 V	400 mA
–24 V	90 mA

2.3. Front panel

The front panel of the Mod. C 205 is shown in Fig. 1.2.

The front panel of the Mod. C 205 A is shown in Fig. 1.3 and differs from that of the Mod. C 205 for the sixteen 00-type LEMO connectors (CHANNEL inputs) instead of the 32+32 pin flat cable-type connector (CHANNEL INPUT connector) mounted on the Mod. C 205.

2.4. External connectors

CLEAR input

Function:
input connector for the CLEAR signal.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications: Std. NIM level signal; high impedance. Width: ≥15 ns.

N.B.: if the CLEAR input is not used, a 50 Ω termination is required.

GATE input

Function:
input connector for the GATE signal.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications: Std. NIM level signal; high impedance. Width: from 100 ns to 5 µs. Timing: the leading edge of the GATE signal must precede the leading edge of the analog input by ≥ 65 ns.

N.B.: It is possible to connect CLEAR and GATE to more than one Mod. C 205 in daisy-chain: the CLEAR and GATE inputs on the last Mod. C 205 in the chain must be terminated by inserting a 50 Ω termination resistor between pins 1 and 2 of the 5+5 pin flat cable type connector for the CLEAR and between pins 9 and 10 for the GATE (see Fig. 2.1, p.10).

TEST input

Function:
input connector for the TEST signal.
Mechanical specifications:
00-type LEMO connector.
Electrical specifications: 470 Ω impedance. Polarity: negative (for all models). In parallel with all channels.

CHANNEL INPUT connector

Function:
input connector for the signals to be converted.
Mechanical specifications:
32+32 pin flat cable-type connector (Mod. C 205; see Fig. 1.2) or 16 LEMO 00-type connectors (Mod. C 205 A; see Fig. 1.3).
Electrical specifications:

Polarity:	either positive or negative or differential, depending on the module version (see Table 1.1).
Impedance:	50 Ω ± 1.5% (Mod. C 205 N, Mod. C 205 P, Mod. C 205 AN and Mod. C 205 AP; see also Table 1.1); 110 Ω ± 1.5% (Mod. C 205 D and Mod. C 205 A; see also Table 1.1).
Voltage range for linear response:	≈ 1.5 V, 100 mV/ns slew rate
Offset voltage:	±4 mV.
Full scale range:	≈ 120 pC (15 bit resolution); ≈ 900 pC (12 bit resolution).

CONTROL connector

Function:
input/output connector, particularly suitable for daisy-chain configurations, to deliver the control signals (CLEAR and GATE) and receive/deliver the BUSY signal. The latter is an OPEN COLLECTOR TTL signal.
Mechanical specifications:
5+5 pin flat cable-type connector (see Fig. 2.1, p.10 for pin assignment).
Electrical specifications:

CLEAR:	CLEAR signal, std. NIM level.
BUSY:	BUSY signal, OPEN COLLECTOR TTL level. It indicates that the conversion is still active. If it is used, the pin 4 of the 10-pin strip header must be pulled-up at +5 V via a resistor (e.g. 1 kΩ) . If several modules are daisy-chained, only one pull-up resistor must be inserted.
GATE:	GATE signal, std. NIM level.
PRO:	(the PRO input signal is used only with the Mod. C296. Please refer to the Mod. C296's manual for details).
GND:	GROUND common terminal.

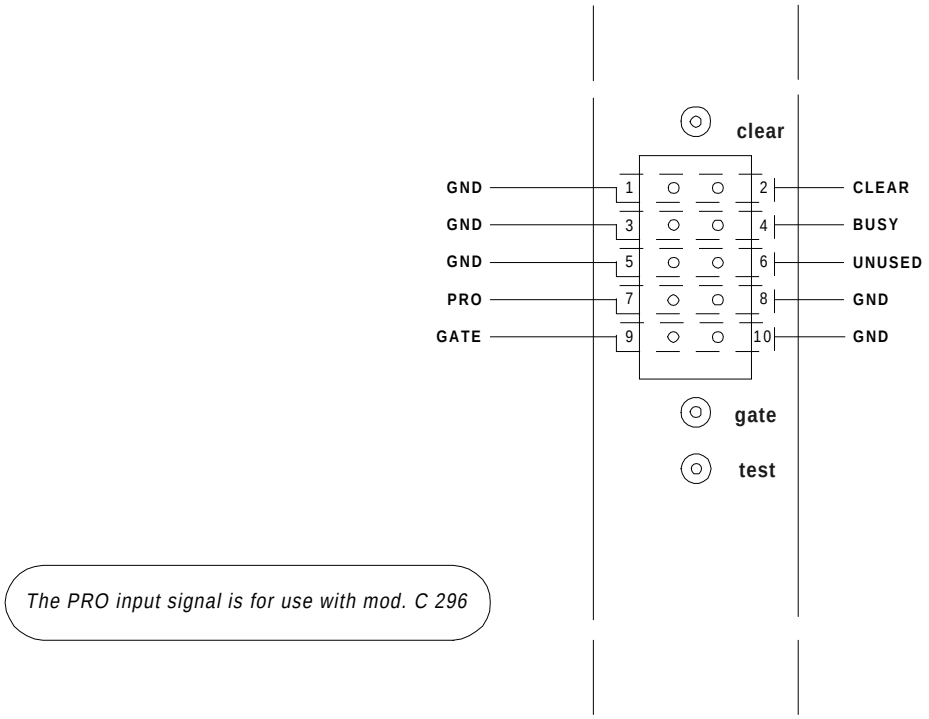

Fig. 2.1 – Output flat cable-type connector: pin assignment

2.5. Technical specifications table

Table 2.1 – Mod. C 205 technical specifications table

Full Scale Range	≈ 900 pC (12 bit resolution) ≈ 120 pC (15 bit resolution)
Conversion gain	≈ 30 counts/pC (15 bit resolution); ≈ 4 counts/pC (12 bit resolution).
Noise	± 1 count max.
Voltage range for linear response	≈ 1.5 V, 100 mV/ns slew rate
Integral non linearity	± 6.5 counts (15-bit resolution); ± 2.5 counts (12 bit resolution).
Interchannel uniformity	2%
Gate width	From 100 ns to 5 µs
Conversion time	1.6 ms per 32 channels.
Fast Clear time	300 ns
Test sensitivity	≈ 300 times the input sensitivity.
Pedestal variation vs GATE width	≈ 50 counts/100 ns (15-bit resolution); ≈ 7 counts/100 ns (12 bit resolution). Adjustable via internal trimmer.
Residual pedestal	For a GATE width of 350 ns and a high impedance source: ≈ 200 counts (15-bit resolution); ≈ 30.counts (12 bit resolution).
Temperature coefficient	+3 counts/C° max

3. CAMAC functions

F(2) N A(0)

Reads the **n-**th memory location and moves to the **(n+1)-**th location. Q response is TRUE for each reading until the 64th included. Q response is FALSE and LAM is cleared at the 65th reading (see below)[1].

PERFORMED FUNCTION	CHANNEL	READS WORD COMING FROM (See § 4.1)	Q RESPONSE	LAM
1st	1	ADC1	TRUE	ON
2nd	1	ADC2	TRUE	ON
3rd	2	ADC1	TRUE	ON
4th	2	ADC2	TRUE	ON
•	•	•	•	•
•	•	•	•	•
63rh	32	ADC1	TRUE	ON
64th	32	ADC2	TRUE	ON
65th	//	//	FALSE	OFF

F(8) N A(0)

Tests the LAM presence. Q response if LAM is true

LAM is set at the end of the conversion, that is ≈1.6 ms after the GATE.

F(9) N A(0)

Resets the module (LAM and BUSY signals are deactivated but the input charge persists). It does not give a Q response.

F(10) N A(0)

Tests and clears LAM. Q response if LAM is true.

Z, C

Same as F(9) N A(0).

[1] For the Mod. C 205 A, which has only 16 channels, the following applies: Q response is TRUE for each reading until the 32th included. Q response is FALSE and LAM is cleared at the 33th reading.

4. Operating modes

4.1. General information

The Model C 205 32-CHANNEL CHARGE-INTEGRATING ADC allows the analog-to-digital conversion of up to 32 independent charge sources. Inputs can be positive, negative or differential, according to the chosen model version (see Table 1.1).

At the end of an external GATE pulse, the charge associated with each input signal is converted into two words:

- a 12-bit word generated by the ADC following the 1X-gain amplifier (ADC1 in Fig. 1.1, p.5);
- a 12-bit word generated by the ADC following the 7.5X-gain amplifier (ADC2 in Fig. 1.1, p.5), corresponding to 15 bit resolution.

Both the words are stored into consecutive locations of a RAM-type memory readable via CAMAC. As soon as the 64th word has been stored a LAM signal becomes true, and the conversion values can be read performing the appropriate CAMAC-function sequence.

4.2. Operating instructions

CAUTION: ***turn OFF the CAMAC crate before inserting or removing the module.***

1. Insert the C 205 module into the CAMAC crate, then turn the crate on.

2. The Inhibit CAMAC line does not have to be set. Perform an F(9) N A (0) CAMAC function or a C or Z CAMAC command: the LAM and BUSY signals are set to false condition.

3. Connect the signal sources to the Mod. C 205 input connector.

4. Connect the "GATE" connector to a signal source (NIM level).

The GATE width can be set in the range from 100 ns to 5 µs.

5. Activate the signals to be converted and the GATE signal: the conversion process begins after the GATE end.

The leading edge of the GATE signal must precede the leading edge of the inputs to be converted by at least 65 ns.

N.B.: When GATE pulses are sent in rapid succession, they may occur during a conversion. To avoid this, never activate the GATE signal during the conversion time (1.6 ms per 32 channels). Use the BUSY output signal (refer to Fig. 2.1, p.10) to inhibit the GATE signal source.

The BUSY is activated (low level) by the external GATE and is reset (high level) by an F (9) N A(0) or by another external CLEAR.

6. In the case that the user wishes to perform a new acquisition before the end of the current conversion, a NIM level pulse (width: ≥15 ns) should be sent to the "CLEAR" connector of the module: any input charge is discharged.

At the end of the conversion the input charge is removed automatically and the converted value (in digital) is memorised in the RAM. In this case, to perform a new acquisition it is sufficient to execute an F (9) N A(0) without forwarding the external CLEAR.

Before the end of conversion only an external CLEAR pulse can remove the input charge. In this case, to perform a new acquisition it is sufficient to send an external CLEAR pulse without forwarding an F (9) N A(0).

The external CLEAR removes the input charge, resets the BUSY and has no effect on the LAM.

The time difference between the trailing edge of the external CLEAR and the leading edge of the subsequent GATE must be at least 300 ns.

7. Perform an F(8) N A(0) CAMAC function until LAM is true (Q response if LAM is true).

8. Perform an F(2) N A(0) CAMAC function for each of the 64 memory locations (Q=TRUE): beginning from channel 1, the two conversion words correlated with each input signal are read.

9. Perform an F(2) N A(0) CAMAC function (the 65th one, Q=FALSE): the LAM signal is deactivated and it is possible to perform another conversion process.

If all the readings are performed it is sufficient to perform an F(9) N A(0) or an external CLEAR before a new acquisition.

If all the readings are not performed the user must perform an F(9) N A(0).

5. Calibrations

The C205 module is delivered fully tested and calibrated from the factory. Adjustment operations are necessary only if repairs have been made in a circuit affecting calibration and if you have reason to believe the unit may be out of calibration.

Calibration settings performed at the factory are optimised for both 12-bit and 15-bit operation with a 100 ns gate width. Therefore, if the user wants to operate the module with different gate widths, further calibration operations may be required by adjusting some of the six internal trimmers (labelled "P1", "P2", "P3", "P4", "P5", "P6" on the module's Printed Circuit Board; refer to Fig 5.1 for their location on the PCB).

The six trimmers together with their relevant function and factory settings are listed in the table below.

TRIMMER	ADJUSTMENT FUNCTION	SETTING VALUE
P1 (*)	Pedestal variation vs GATE width.	7 counts/100 ns
P2 (*)	GATE and CLEAR voltage level corresponding to logical 1	15 V
P3 (*)	GATE and CLEAR voltage level corresponding to logical 0	5 V
P4 (**)	Counts offset (12 bit resolution)	≈ 50 counts
P5 (**)	Counts offset (15 bit resolution)	≈ (50×7.5) counts
P6(**)	Common offset (12 bit and 15 bit range)	

CAUTION: do not modify the setting of the P2 and P3 trimmers; otherwise, the module can be damaged!

(*) A counterclockwise rotation increases the set value.

(**) A clockwise rotation increases the set value.

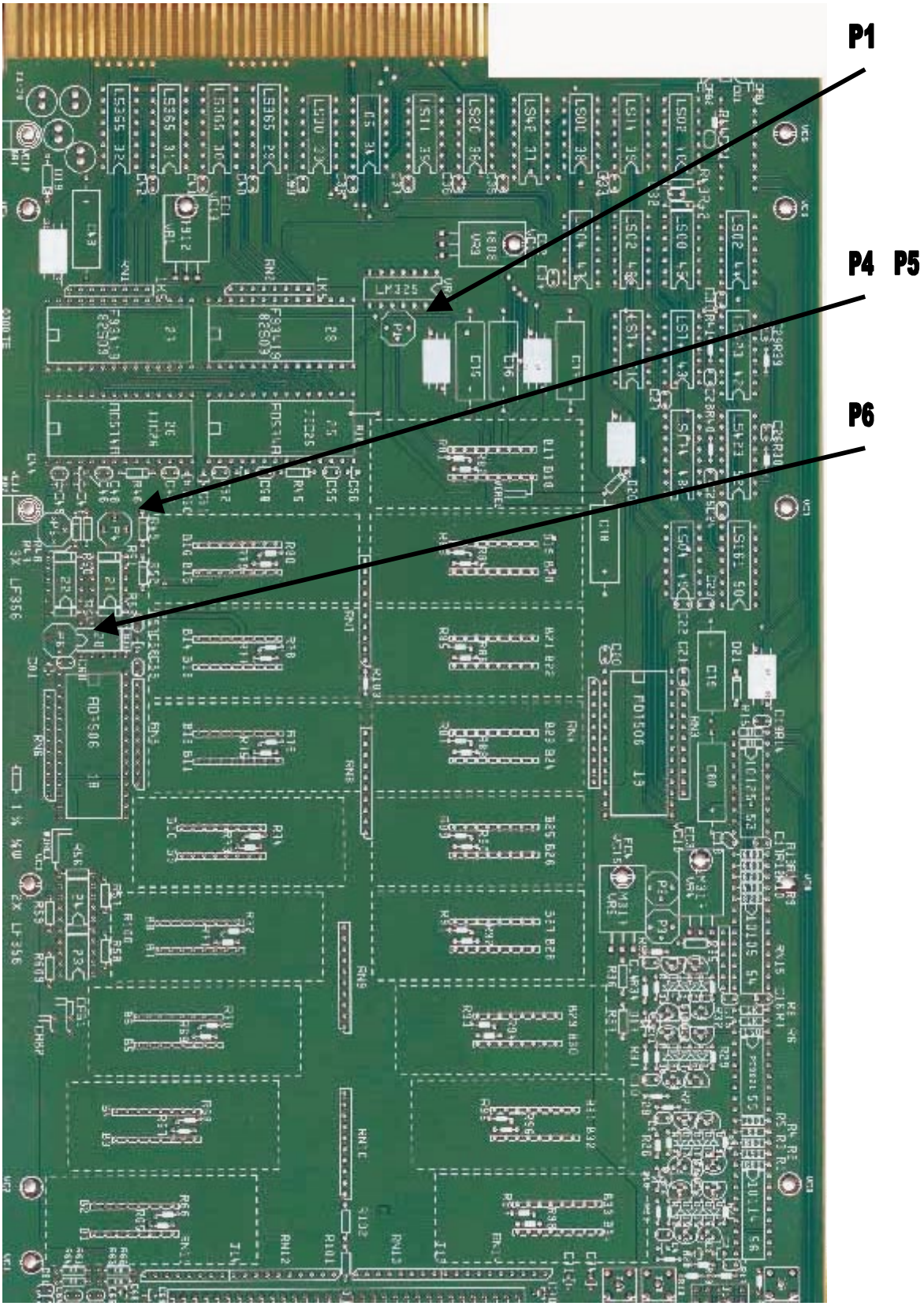

Fig. 5.1 – PCB layout