Technical Information Manual

MOD. N 113

DUAL 12 INPUTS
OR

30th August 1991

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CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

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DESCRIPTION

Model N 113 is a 1-unit wide NIM module including two identical sections , A and B, each one performing the logic function "OR" on its 12 inputs.

The output of each section can be always enabled (pos. GATE OFF), or by the GATE input (pos. GATE ON) according to the position of the front-panel switch.

With 4 internal jumpers the module can be converted to a single 24-input "OR", with separate or common gate control.

SPECIFICATIONS (each section)

INPUT CHARACTERISTICS

Inputs ..... 12; 50 Ω impedance; std. NIM levels; DC coupled

Minimum Pulse Width .... 7 ns

GATE Input ..... 1; 50 Ω impedance; std NIM levels; DC coupled.
Enabled by the front-panel switch.

Min. GATE Pulse Width .. 7 ns

OUTPUT CHARACTERISTICS

Output ..... 2 identical; 50 Ω impedance; std. NIM levels.

Rise-Fall Time ..... ≤ 3 ns

Four internal jumpers allow to condition the outputs to different configurations of the two gates.

GENERAL CHARACTERISTICS

Input - output delay ..... ≤ 10 ns

All connectors are **LEMO 00** type

Power requirements: -6V 510 mA

OUTPUT FUNCTIONS

According to the position of the jumpers P1, P2, P3, P4 the module can deliver different output signals. See fig. 1 .

1) To perform on sections A and B the logic OR of the respective 12 input signals :

   P1, P2, P3, P4 OFF

2) To perform on sections A and B the logic OR of the respective 12 input signals enabled with the respective GATE signals :

   P1, P2 OFF P3, P4 ON

   The GATE switches must be ON

3) To perform on section A the logic OR of its 12 input signals enabled with the GATE B signal and on section B the logic OR of its 12 input signals enabled with the same GATE B signal :

   P1, P3 OFF P2, P4 ON

   The GATE B switch must be ON

4) To perform on section A the logic OR of its 12 input signals enabled with the GATE A signal and on section B the logic OR of its 12 input signals enabled with the same GATE A signal :

   P1, P4 OFF P2, P3 ON

   The GATE A switch must be ON

5) To perform on sections A and B the logic OR of the respective 12 input signals enabled with the logic AND of the GATE signals :

   P1 OFF P2, P3, P4 ON

   The GATE switches must be ON

6) to perform on sections A and B the logic OR of all the 24 input signals :

   P2, P3, P4 OFF P1 ON

7) To perform on sections A and B the logic OR of all the 24 input signals enabled with the respective GATE signals :

P2 OFF P1, P3, P4 ON

The GATE switches must be ON.

8) To perform on sections A and B the logic OR of all the 24 input signals enabled with the GATE B signal :

P3 OFF P1, P2, P4 ON

The GATE B switch must be ON.

9) To perform on sections A and B the logic OR of all the 24 input signals enabled with the GATE A signal :

P4 OFF P1, P2, P3 ON

The GATE A switch must be ON.

10) To perform on sections A and B the logic OR of all the 24 input signals enabled with the logic AND of the GATE signals :

P1, P2, P3, P4 ON

The GATE switches must be ON.

TEST PROCEDURES

Necessary instruments:

- Pulse generator NIM std. output (N 2255B).
- Delay unit (N 146, N 107, N108).
- Fan-out unit (N 105, C 104).
- Oscilloscope Tektronix Mod. 475A or equivalent.

1) Select via P1, P2, P3, P4 jumpers the output function explained at point 1) of the previous paragraph .

2) Feed the first input connector of the A section with a compatible signal to the input specifications (i.e.100 nsec.width) .

3) Verify that the output signal is the same as the input one independently from the GATE switch position .

4) Repeat point 3) for all the A and B section inputs .

5) Feed all the A section inputs with 12 identical signals delayed each other by the same delay and verify that the output signal width is the sum of the input width and the 12 delays .

6) Repeat point 5) for the B section .

7) Select the output function at point 2) of the previous paragraph .

8) Feed the GATE inputs.

9) Selecting the 3) or 5) condition ,verify that the output signal is the logic AND of the input signal(s) and the gate(s) signal for the A and B section.

10) Repeat points 8) and 9) for the 24 inputs logic OR.

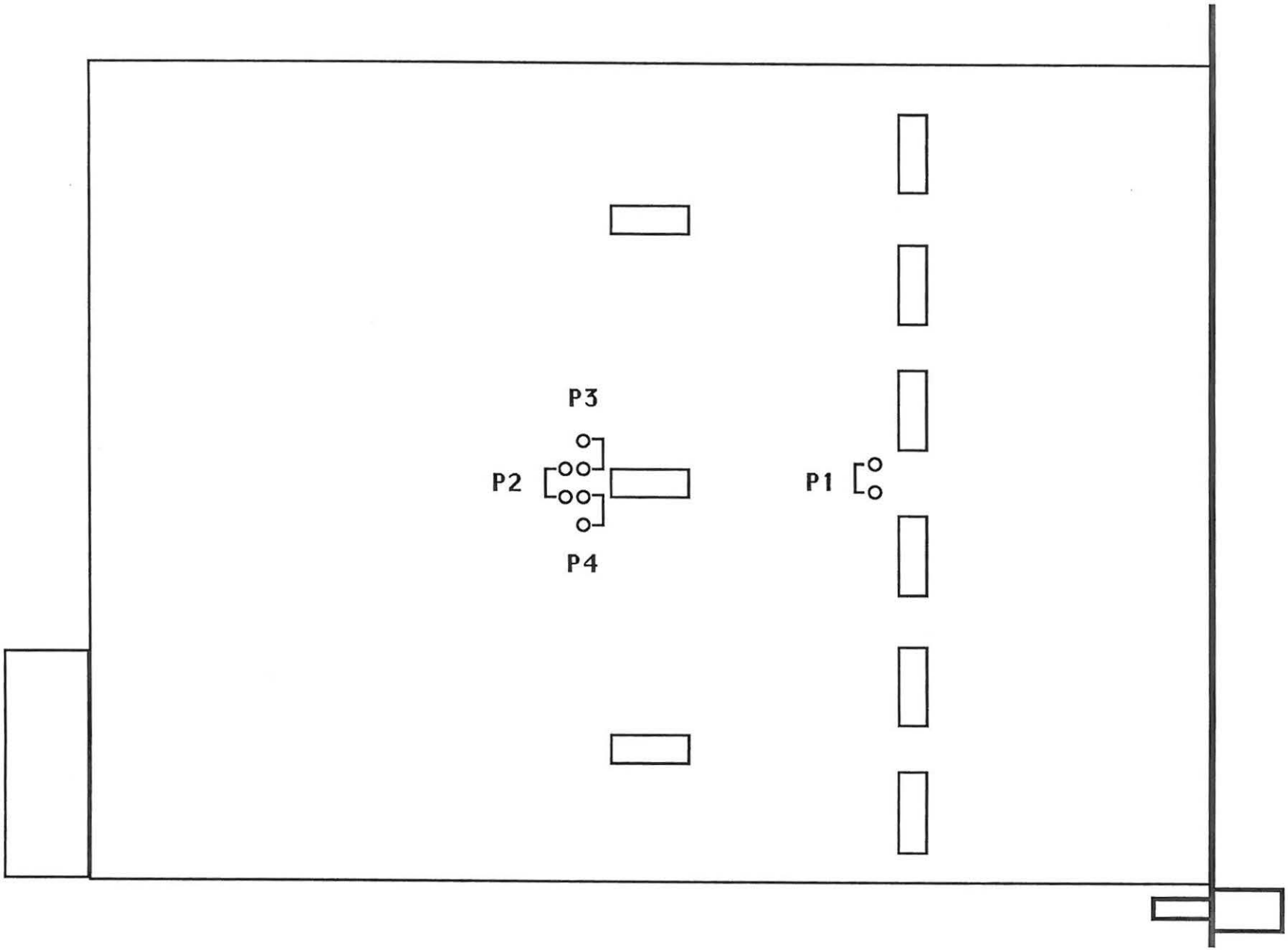

Fig. 1